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IMPROVED PROGRAM VIEWING APPARATUS AND METHOD

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BACKGROUND OF THE INVENTION

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Field of the Invention

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This invention relates to the field of delivery of programming, for example entertainment and educational programming such as that currently delivered by television and film technology. The application is a continuation-in-part of our prior application U.S. 08/322,069 filed October 12, 1994 for a Frequency Convertor System, the contents of which are incorporated by reference.

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Description of the Prior Art

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In the Prior art it is known to deliver programming such as entertainment and educational programming by physical shipment of films and magnetic recording, terrestrial transmission of television signals via wires or fibers, transmission of radio frequency energy via satellite or otherwise. In particular, it is known to transmit multiple channels of television programming utilizing compressed digital or analog data over satellite and cable television systems. For all of these modes of transmission a user may typically either view the program as it is transmitted or may record a single transmitted program for later viewing. With present technology, however, it is normally required to have available one recorder for each transmitted program. Some in the prior art have attempted to develop a frequency converter system that would allow this to change with varying degrees of success.

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Although some of these frequency converter systems functioned properly, many of these frequency converter systems

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1 were excessively complex and costly to manufacture. Accordingly,
2 the frequency converter systems of the past have not found wide
3 use in the media art.

Frequency converter systems of the prior art include U.S. Patent 4,829,257 to J. Carl Cooper for an Improved Device for Accurately Phase or Frequency Shifting an Input Signal. This invention essentially incorporated a variable resistor extending between at least two known phase shifted values of the input signal. U.S. Patent 4,868,428 to J. Carl Cooper discloses an Apparatus and Method for Accurately Shifting the Phase or Frequency of a Complex Signal. U.S. Patent 5,097,218 to J. Carl Cooper discloses an Apparatus and Method for Accurately Multiplying the Phase or Frequency of Complex Time Varying Signals by a Given Factor Which May be Non-integer. The contents of these patents are incorporated by reference.

OBJECTS OF THE INVENTION

It is an object of the invention to provide an improved program delivery apparatus and method which is compatible with existing program delivery systems and provides the user with improved access to such programming. In particular, as described below, it will be possible for each user to select and view one and/or multiple programs virtually at random (within the limits of storage availability) whenever he desires. In addition, it will be possible for a user to stop or suspend viewing in the middle of a program (such as to accommodate interruption by a phone call which may also be provided by the present invention) and to continue viewing after the interruption without missing any of the program. During the time the viewer is occupied with the phone call the incoming program would be recorded. Further, the user can manually and/or automatically accelerate programs to accommodate for the time

1 lost and/or otherwise compensate for time without objectionable
2 artifacts. In addition, previously stored programs may be viewed
3 at accelerated (or decelerated) speed, or repeated or portions
4 reviewed, all upon the viewers wish, via the frequency convertor
5 for example or otherwise.

6 This system provides a user with the ability to change
7 the frequency of the produced signal by a percentage function
8 based on the ratio between the lengths of time of production.
9 Alternately the user can change the frequency of a real time
10 signal (i.e., without altering the time period of production).
11 For example, it might be desirable to replay a prerecorded thirty
12 (30) minute television program in a time duration of twentyeight
13 (28) minutes in order to fit a time slot without the associated
14 seven percent (7%) increase in frequency. The replay of a
15 prerecorded thirty (30) minute television program in twenty seven
16 (27) minutes would allow alternately for the three (3) minutes of
17 phone calls or other activities during the program. The present
18 invention also allows shows to be expanded to fit time slots.

19 In another example, entertainment or educational pro-
20 grams or movies could be presented in shorter time to reduce the
21 operating costs or to allow more movies to be shown in ^{an} evening.
22 A similar advantage could be realized in the replay of
23 prerecorded music or voice on a radio station. Messages from an
24 answering machine could also be accelerated, perhaps greatly, for
25 rapid playback while retaining normal voice frequencies. Again,
26 the present invention allows this without the pitch shift
27 artifacts that would otherwise be ascertainable to the consumer.
28 Another example would be to lower the occupied bandwidth of a
29 signal to be transmitted over a radio propagation or other
30 transmission medium. This is a major thrust of this present
31 invention. In this specification, the data may be fed into a
32 large memory (for example 4-5 gigabytes), perhaps intermittently,

1 at one speed and fed out at a second (normally slower and perhaps
2 constant) speed, thus facilitating signal presentation and/or
3 data operations. Another object of the present invention is to
4 provide an improved apparatus and method for frequency conversion
5 capable of decreasing or increasing the time base of a signal
6 without a significant change in frequency. Another object of the
7 present invention is to provide an improved apparatus and method
8 for frequency conversion capable of a significant decrease or
9 increase of the time base of a signal without significant change
10 in perceptible frequency.

Another object of the present invention is to provide an improved apparatus and method for frequency conversion capable of use with a computer based storage and retrieval system of prerecorded programs or information. A further object of the present invention is to increase the reproduction utilization capabilities of video and audio recorders, movies and films, answering machines, voice mail boxes, and other signal storage systems. Other objects and a fuller understanding of the invention may be had by referring to the following description and claims, taken in conjunction with the accompanying drawings, in which:

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a diagram of the preferred embodiment of the invention.

26 Figure 2 shows a diagram of a prior art MPEG 2
27 Development system.

Figure 3 shows a diagram of the preferred embodiment of the User Remote of the invention.

Figure 4 shows a program recording priority spread sheet form of the present invention.

1 Figure 5 shows the spread sheet of Figure 4 with
2 typical user entries.

3 Figure 6 shows a diagram of the Data Manager and Data
4 Storage portions of the invention.

5 Figure 7 is a block diagram of the theory of the
6 frequency conversion;

7 Figure 8 is a block diagram illustrating an improved
8 frequency converter system connected to an example input signal
9 having a first frequency sustained for a first length of time for
10 generating an example output signal having substantially the same
11 first frequency sustained for a second length of time;

12 Figure 9 is a graph illustrating a single cycle of an
13 example input analog signal at a first frequency;

14 Figure 10 is a graph illustrating a translation of
15 the single cycle of the input analog signal of FIGURE 8 into
16 digital form;

17 Figure 11 is a graph illustrating the selection of a
18 digital sample for the signal of FIGURE 9;

19 Figure 12 is a graph illustrating the addition of a
20 duplicate of the selected digital sample from the samples of
21 FIGURE 10 to provide a sample digital form of a modified output
22 signal;

23 Figure 13 is a graph illustrating a type of linear
24 interpolation of the signals of FIGURE 11;

25 Figure 14 is a graph illustrating a transformation of
26 the digital samples of FIGURE 12 into an output analog signal;

27 Figure 15 is a graph comparing a single cycle of the
28 input signal of FIGURE 8 and the output signal of FIGURE 13;

29 Figure 16 is a graph setting forth the output signal
30 of FIGURE 13 as actually perceived by the consumer due to its
31 production at a higher reproduction rate than the input signal of
32 FIGURE 8;

1 Figures 17-18 are drawings demonstrating the sampling
2 and nature of signals;

3 Figures 19-21 are figures like FIGURES 11-13 showing
4 an example deletion of a digital sample;

5 Figure 22 is a detailed block diagram of a frequency
6 converter system;

7 Figure 23 is a graph comparing a first signal and a
8 second signal and illustrating the reset of the phase angle of
9 the signals at a common zero crossover;

10 Figure 25 is a figure like FIGURE 23 illustrating a
11 reset at the top of a signal waveform;

12 Figure 24 is a graph of the constant, non-reset first
13 signal in FIGURES 23 and 25;

14 Figures 26-27 are circuit diagrams of example frequency
15 converter systems;

16 Figures 28-29 are block circuit diagrams of a MPEG
17 implementation of the invention;

18 Figure 30 is a block circuit diagram of a multiple
19 channel device;

20 Figure 31 is a block diagram of a circuit for signal
21 playback;

22 Figure 32 is a series of representational block
23 diagrams setting forth an example resetting of memory lines in an
24 expansion or contraction frequency conversion device; and,

25 Figure 33 shows an adaptive filter network for
26 incorporation into the system of FIGURE 31.

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28 DESCRIPTION OF THE PREFERRED EMBODIMENT

29 Figure 1 shows a diagram of the preferred embodiment of
30 the invention as used in a home or business environment. Figure
31 1 includes an example programming source and delivery channel
32 which provide program and/or data material over a delivery

1 channel, a delivery channel interface coupled to the delivery
2 channel and operable to receive said program material and/or data
3 therefrom and provide said program material and/or data in a
4 stream to a data manager including a program data processor and a
5 program data storage, said data manager being coupled to the
6 program data storage to store selected portions of the program
7 material and/or data in the program data stream, with the data
8 manager also preferably coupled to a removable data storage to
9 store selected portions of the program material and/or data in
10 the program data stream or previously stored program material
11 and/or data from the program data storage on a removable media,
12 and with the data manager also coupled to a user display via a
13 program data processor to retrieve and/or access program material
14 and/or data from the program data storage, removable data storage
15 and/or program data stream or a combination thereof to provide
16 and/or access program material and/or usable data to a user such
17 as a user display including a computer, with said user display
18 being coupled to a user remote whereby the user may interactively
19 program and control the data manager and other components in
20 order to select, control and/or utilize the program and/or data
21 being accessed. The data manager also is coupled to an alternate
22 user display which is coupled to an alternate user remote which
23 allows the same and/or other program material to be displayed
24 and/or utilized including separately from the first user.

25 It will be understood from the teachings herein that
26 multiple delivery channels, delivery channel interfaces, program
27 data streams, program data processors, user displays, computers,
28 and user remotes may be utilized individually or in combinations
29 as desired to provide control and/or multiple operations with
30 multiple programs or users. For purposes of the present
31 disclosure, the following terms are given the following
32 definitions which are somewhat broader than the definitions

1 normally associated with the term.

2 Program is the information having some intrinsic

3 value which is of use or interest to a person, being or thing.

4 Program shall encompass both normal information such as commonly

5 known entertainment programs (for example movies and live

6 television programs), informational programs (for example

7 commercials and educational classes) and any other information

8 including of an audio, video, text, data or natural type which

9 may be of value to a particular user. Program includes singular

10 information, multiple information, and combination information.

11 Programming takes on two meanings: the first is the

12 creation, generation, providing or distribution of one or more

13 program and/or data streams, the second is the programming of the

14 operation of the invention and its usage and/or access of the

15 programs. The meaning being used will be apparent from the

16 context.

17 User is the person, being, thing, facility computer, or

18 location which receives and/or uses one or more program. User

19 may be referred to as a location, i.e. the User Location. There

20 is no requirement that there be only one user, or that a user who

21 operates the invention be the same user who utilizes the program.

22 There may be multiple simultaneous or sequential users.

23 Additionally, the program data stream and/or program data storage

24 may be considered a user in that it may automatically operate the

25 invention to provide information which the invention utilizes to

26 determine the need ^{and/or} priority for storing or displaying a

27 program. There may be another user who is a person simultaneously

28 watching or utilizing a stored program.

29 Viewing is the use of information by the user and shall

30 include visual use, auditory use, computer use and/or virtual use

31 as will be apparent from the context in which the term is used.

32 Viewer is a user which is viewing.

1 Display is the presentation of information for possible
2 utilization, for example by viewing (that is seeing and/or
3 listening) or processing (that is utilizing at a then non-
4 recognizable level). User Display is the presentation and/or
5 utilization of information for possible utilization primarily by
6 the User, for example by viewing, which information may also be
7 utilized by others.

8 Data shall apply to the information of any nature
9 carried or stored by the media, channel or interface and will be
10 recognized by one of ordinary skill in the art to take on
11 different forms including programs as will be apparent from the
12 context of the usage.

13 Channel is used both in the communications theory sense
14 where it applies to the means or mechanism by which data is
15 stored, transmitted or delivered, and is also used in a program
16 sense such as conventional television channel sense where it
17 means a traditional broadcast, cable, satellite or tuner channel,
18 which usage will be apparent from the context.

19 Key is an actuator or circuit suitable for interface
20 with and/or operation by the user. Key Label is an identifier
21 associated with a Key and which is preferred to be recognizable
22 by the user.

23 In Figure 1, programming is provided at a source by any
24 of the known methods for actual programs and/or data, such
25 methods including optical disk, magnetic disk, film, recordings,
26 electronic memory, hard drives, etc.

27 For the preferred embodiment, a television video file
28 server such as the Hewlett Packard video file server available
29 from Hewlett Packard of Palo Alto, California is utilized. It is
30 preferred that the program for this example system consist of
31 television video, multiple audio and ancillary data including
32 closed captioning, time code, presentation time stamp and program

1 schedule information such as those commonly known in the art
2 and/or primary data. *The program is preferred*
3 simultaneously provided programs and/or data. The programs of
4 this preferred example system are preferably compressed or
5 redacted, for example according to the ~~MPEG 2~~ standard, and
6 coupled to N multiple delivery channels for satellite or other
7 transmission over a large area of land whereby it may be received
8 by numerous users, all as commonly known in the art.

9 Although such programming services and delivery
10 channels are commonly known in the art, it will be suggested
11 herein that these commonly known facilities may be modified to
12 further accommodate the present invention. For example, at the
13 User location, the transmitted programs are received by one or
14 more delivery channel interfaces which couple to the N particular
15 delivery channels and provide O program data channels, where N
16 and O are numbers represent 1 or more and need not be the same.
17 It is preferred that all of the associated data for each of the
18 programs be provided on a single MPEG 2 compressed data stream
19 out of the delivery channel interface from which the data is
20 recovered, for example all of the television video, multiple
21 audio and ancillary data including closed captioning, time code,
22 presentation time stamp and program schedule information for a
23 particular program be carried together on a single MPEG 2 format
24 program data stream.

25 The O program data streams are coupled to a data
26 manager having one or more associated program data processors.
27 The data manager is preferred to operate to store all of the O
28 program data streams in a program and other data storage device
29 as the data streams are presented. It is preferred that the data
30 storage device have a random access capability such as that
31 provided by semiconductor, magnetic or optical storage
32 technologies, such as known computer industry RAM, hard disk and

1 optical disk drives. The data storage device could also have
2 sufficient speed and memory to capture all incoming programming
3 for later individual non-real time processing. It will be
4 recognized that there is no requirement as to the data rate or
5 regularity or speed of transmission of programs, although it is
6 preferred that the Data Manager and Program Data Storage operate
7 to receive and store program data as it received.

8 It should be pointed out that with a finite amount of
9 program data storage capability, sooner or later there will be no
10 more storage available for incoming programs. When that event
11 occurs or when it is identified that that event is nearing
12 occurrence, the Data manager is preferred to be previously
13 programmed to start losing or discarding known previously stored
14 data or data types according to a known set of priorities. It
15 will be noted that the known set of priorities may be changed
16 from time to time as will be described below. Upon the
17 identification of no more storage being available for incoming
18 programs, and the possible resultant loss of previously stored
19 data, it is preferred that overwriting occur based on the amount
20 of remaining storage and the rate of desired incoming program
21 data, based on parameters and priorities which may be selected by
22 one or more chosen user. In this respect, it is preferred that
23 any multiple viewers are to be given priority such that a higher
24 priority user's inputs are performed at the expense of a lesser
25 priority user's inputs in the event both can not be accommodated.
26 As an example, the user could ^{choose} to store all of the programs
27 from a particular program, network or service (for example a news
28 program or data stream) while ignoring, overwriting or not
29 storing another particular program, network or service (for
30 example a court room television channel). As an additional
31 feature, the user may direct the Data Manager to keep memory
32 available for a particularly desirable program, network or

1 service, and/or to only store a given quantity of one or more
2 program network or service. For example, the user may direct the
3 Data Manager to only store the last three days worth of
4 channel A, the last four programs of program B, none of program
5 C, none of channel D and to always store programs of type E.
6 Quantities may be chosen in units of time, programs, elements of
7 a series or according to program, channel, network or service
8 content or combinations thereof. It will be recognized that such
9 complexities tend to create exponentially growing requirements on
10 the Data Manager with each additional parameter, such capability
11 is still well within the abilities of current programming and
12 computer operation capabilities of those of ordinary skill in the
13 art. Additionally, it will be recognized that a Removable Data
14 Storage capability (in addition or separately) may be required or
15 desirable with the user having the ability to direct the Data
16 Manager to cause a known program or programs to be stored thereon
17 either from the Program Data Storage, or directly from the
18 Delivery Channel Interface. The Removable Media may then be
19 physically removed and/or replaced - for example for storage for
20 archive purposes or to be moved to other locations.

21 The selection of such program or programs may also be
22 subject to the same or different selection requirements and
23 priorities, as the program data which is stored on the Program
24 Data Storage. Program data from removable Data Storage Media may
25 also be read therefrom for example via media previously archived
26 or received from other locations. The Data Manager & Program Data
27 Processor(s) also couple to one or more User Display which is
28 preferred to be a video CRT, LCD or Active Matrix type display
29 and associated audio transducer such as a speaker set or
30 headphones. Each User Display also couples to a User Remote which
31 is preferred to be a keypad or keyboard which is preferably
32 wirelessly bidirectionally coupled thereto, such as by infrared

1 beams. It is preferred that the User Remote additionally have the
2 capability to program and reprogram the keys thereon, in order
3 that a small number of keys may perform multiple functions,
4 and/or in order that the user may chose convenient key labels for
5 the keys which facilitates the viewers identification and use
6 thereof.

7 It will be recognized that it will also be useful for
8 the User Remote to contain a message display, for example such as
9 an LCD readout, beeper or speaker, which allows the user to
10 receive messages directly or indirectly from other parts of the
11 system without having to receive them from the User Display.
12 This is especially useful for Human viewers where an audible
13 signal would aid in locating the remote or signaling invalid
14 operation, and an LCD display would allow messages to be
15 displayed during programming type operations without requiring
16 the user to look away from the remote. It is desired that the
17 Data Manager also include one or more Program Data Processor
18 which function to convert the MPEG 2 format program data stream
19 from the Delivery Channel Interface, Program Data Storage and/or
20 Removable Data Storage into a format which may be displayed on
21 the User Display. In addition, it is preferred that the Program
22 Data Processor provide capabilities for displaying multiple
23 programs on the User Display, such as can be provided by
24 displaying different programs in multiple windows on a CRT type
25 video display, and for providing special effects such as spatial
26 manipulations or enhancement of images or of sounds and quick
27 viewing and time compression (or expansion) capability, for
28 example such as that described in copending U.S. Patent
29 Application serial number 089,904. Also, it is seen in Figure 1
30 that the Data Manager may be coupled to Other Services, for
31 example such as telephone wire, fiber and other terrestrial
32 communications, remote video cameras, alarms and actuators, such

1 as baby room monitors and doorbells.

2 Communications with the Programming Services which
3 operate the Programming Sources to provide the Programs over the
4 Delivery channels is an important capability provided by the
5 Other Services. In this fashion account charges and payments may
6 be made at the Users wish, for example to automatically arrange
7 for payment for pay per view or other special programs.

8 Of special importance is the ability to interface with
9 program guide services which provide information on upcoming
10 programs. In this fashion, the Data Manager may display lists or
11 charts of upcoming programs along with other program information
12 thereby allowing the User to select wanted ones of the upcoming
13 programs for storage. It will also be noted that many times such
14 upcoming program information is carried as embedded information
15 on the Program Data Streams themselves, thus the Data Manager may
16 acquire this information directly from the data stream.

17 The components used to practice the invention of Figure
18 1 are individually available to one of ordinary skill in the art.
19 The components may be procured and interconnected by one of
20 ordinary skill without undue experimentation or further invention
21 by resorting to the teachings herein taken in accordance with the
22 prior art. For example, the Programming Source may be provided by
23 the aforementioned Hewlett Packard video file server and the
24 DiviCom MPEG-2 Encoder, MPEG-2 ReMultiplexer operating with the
25 DiviCom MPEG-2 System Controller available from DiviCom, Inc. of
26 Milpitas, California. The Delivery Channel Interface may be
27 provided with one or more standard receiving devices well known
28 in the industry, for example a standard satellite DSS tuner such
29 as manufactured by Thompson under the RCA brand name in
30 Indianapolis IN. Data storage by the Program Data Storage and
31 Removable Data Storage is preferred to be provided in a single
32 unit which operates with removable writable optical discs. These

1 functions may be separated however if desired, for example to
2 utilize lower cost storage such as computer hard disks or faster
3 semiconductor memory for the Program Data Storage. The Program
4 Data Storage may be provided for analog or D1 video and audio by
5 the RAMSES video ram recorder available from EVS Broadcast
6 Equipment of Lie'ge Belgium or by the DLC-V500 available from
7 Pioneer of Long Beach CA. The DLC-V500 utilizes removable optical
8 discs for storage and may also provide the Removable Data Storage
9 either as a separate unit or in combination with the Program Data
10 Storage combined in a single unit. Both the Program Data Storage
11 and the Removable Data Storage may also be implemented for
12 storing the MPEG-2 compressed program data stream with standard
13 computer storage technology, computer hard drives and optical
14 WORM drives respectively. Decoding of the MPEG-2 data stream from
15 any of the sources may be performed with the DiviCom companion
16 consumer, commercial or professional decoders, and provide stan-
17 dard analog or digital video signal(s) for use by the User
18 Display or the RAMSES recorder. The technology for the User
19 Display and infrared technology for communications with the User
20 Remote are commonly available in consumer ⁺Television sets. The
21 Data Manager and communications with the User Display may be
22 implemented with a personal computer such as any of the common
23 multimedia Pentium based computers or a VME bus computer such as
24 the Sun Sparc. Video interface and Digital Signal Processing
25 boards which may be used to implement the Program Data Processor
26 are available from numerous DSP companies including Atlanta
27 Signal Processors, Inc. of Atlanta GA., Ariel Corporation of
28 Highland Park, NJ, Analogic Corporation of Peabody, MA, and
29 Traquair Data Systems, Inc. of Ithaca, NY. Interface cards to
30 interface the computer to the other services are readily
31 available, for example the IBM WindSurfer Communications Adapter
32 from IBM Corporation, Research Triangle Park, NC.

1 Figure 2 shows a prior art MPEG-2 development system
2 which may be used by those who wish to implement and practice the
3 invention on existing hardware with suitable modifications. The
4 C-Cube MPEG 2 Development system available from C-Cube
5 Microsystems of Milpitas Ca. provides a Sun Microsystems Sparc
6 plug in card (VME bus) which provides analog or D1 digital video
7 input, analog video out, stereo analog audio in and out, control
8 of external devices (such as an HP video file server or EVS
9 RAMSES) via RS232 port, user keyboard, full color monitor,
10 storage of MPEG encoded Video on both hard drive and removable
11 tape drive via SCSI bus, Ethernet communications and serial MPEG
12 data communications. To practice the invention, one adds the
13 necessary programming, wireless communication and the User
14 Remote, which may be achieved via the RS232 serial port or
15 Ethernet, and to connect an MPEG program data stream from the
16 Delivery Channel Interface via the serial MPEG data port. Similar
17 development systems are available from other manufacturers.
18 Programming of the hardware operation is provided via the
19 keyboard and will be well within the capabilities of one of
20 ordinary skill in the art from the teaching herein.

21 Figure 3 shows a diagram of the preferred embodiment of
22 the User Remote of the invention. While the User Remote is shown
23 in its preferred embodiment form for use by a person speaking
24 English, it will be understood that it may be modified as
25 appropriate to accommodate persons speaking other languages, or
26 with various handicaps, or to operate with mechanical, electronic
27 or optical interfaces, the latter being particularly well suited
28 for interfacing with other devices. The preferred User Remote of
29 Figure 3 contains an infrared transmitter and infrared receiver
30 for communications with the User Display or other components of
31 the invention by way of infrared light beams, an LCD display and
32 video imager for visual interaction with the user, the video

1 imager for imaging scenes or materials which the user points the
2 imager to and the LCD display for displaying text messages,
3 graphics or images to the user, programmable keys A, B, C, and D
4 each having a programmable label A, B, C, and D, respectively, an
5 audio transducer consisting of a speaker and microphone for audio
6 interaction with the user, up and down keys ~~for communicating~~
7 the users desire to increase or decrease a particular
~~function, Configurable~~
8 ~~function, configurable~~ function keys F1, F2, F3 and F4 with
9 associated configurable labels, and a standard 12 key numeric
10 keypad. The standard 12 key numeric keypad is preferred to be
11 fixed in programming and configuration, and to have nonchanging
12 labels, however if it is desired to facilitate more extensive
13 capabilities the keypad may also be programmable or configurable,
14 and have associated changeable labels.

15 In operation, the user stimulates or actuates the
16 various keys and sensors in proper sequence and combination in
17 order to direct the Data Manager and other components of the
18 system to perform in a fashion to present to the user the desired
19 program material and/or access desired information on the User
20 Display or User Remote. It will be recognized that the Data
21 Manager is capable of communicating with the User Remote to both
22 configure the programmable keys A-D and program their associated
23 labels accordingly, as well to display any desirable messages on
24 the LCD display or couple any desirable sound to the audio
25 transducer. In this fashion the User Remote may function to
26 operate, via the User Display and Data Manager, all needed system
27 functions. It is also recognized that the User Remote may
28 operate directly with other system components to perform wanted
29 functions. As an example of the preferred operation of the User
30 Remote in the present invention, in normal operation key A is
31 labeled sound, and when the operator actuates the A key the
32 message "UP FOR LOUDER-DN FOR SOFTER" appears on the LCD display.

1 By actuating the UP or DN key the operator controls the sound
2 level. Similarly, the B key is used to change the channel up or
3 down, the C key is used to speed up or slow down the playback
4 speed of previously stored programs, and the D key is used at the
5 first actuation to temporarily stop the playback of the program
6 (this operates with program from the data stream or previous
7 storage as will be discussed below) and at the second actuation
8 to continue the program from where it stopped. Similarly, the
9 programmable function keys normally operate with F1 being used to
10 initiate or answer phone (or video phone) calls, much like
11 lifting the handset on a standard telephone, F2 to replay
12 previously stored phone messages much like pressing the play
13 button on a standard answering machine, F3 to select programmable
14 attribute menus for configuring the operation of the system and
15 F4 for selecting programmable display functions of the User
16 Display. Function key F4 operates to inform the Data Manager to
17 display graph functions for COLOR, HUE, BRIGHTNESS and CONTRAST
18 on the User Display, or alternatively on the User Remote LCD. In
19 addition, keys A-D and their labels are reconfigured to
20 indicate COLOR, HUE, BRIGHTNESS and CONTRAST, with adjustment of
21 the particular function desired performed by actuating the
22 associated key followed by the UP or DN key. A second press of
23 the F4 key operates to inform the Data Manager to display graph
24 functions for frequency equalization of the audio reproduction on
25 the User Display, or alternatively on the User Remote LCD. In
26 addition, keys A-D and their labels are reconfigured to indicate
27 they are in use for the functions of left to right and front to
28 back balance of the sound channels. Adjustment of the frequency
29 response is performed by actuating the numeric key associated
30 with the desired frequency to be adjusted (as indicated on the
31 graph display), followed by the UP or DN key.

32 Function key F3 operates to inform the Data Manager to

1 display the first level menu selections on the User Display or
2 User Remote, and to reconfigure appropriate programmable keys and
3 associated labels accordingly. It may be noted that it is
4 preferred that one of the menu selections will be to display
5 menus on the User Display or User Remote LCD or both. After all
6 key actuations, it is preferred that a timer be started which
7 will return the User Display and User Remote to the previous
8 operation 10 seconds after the last key press, in order to resume
9 normal displays. Alternatively, one or two of the programmable
10 keys may be programmed to perform CANCEL or END functions.

11 Figure 4 shows the spread sheet of the preferred first
12 menu available under the F3 key, this menu allows the operator to
13 select individual incoming program data streams to be stored or
14 ignored and their method of display. For purposes of explaining
15 the instant invention it will be assumed that there are four
16 incoming data streams corresponding to four programming services
17 or networks which provide SPORTS HOBBIES NEWS and MUSIC. Other
18 data streams could also be utilized.

19 The User Display or User Remote LCD lists a spread
20 sheet type display with the left most entry being the Program
21 Data Stream Number with vertical columns for IDENTIFIER, PROGRAM
22 STORAGE TIME 1, STORE PERIOD, MOST/LEAST RECENT OVERWRITE,
23 STORAGE TIME 1 PRIORITY, PROGRAM STORAGE TIME 2, STORAGE TIME 2
24 PRIORITY, STORE PERIOD, MOST/LEAST RECENT OVERWRITE. If desired,
25 additional entries may be provided for.

26 The IDENTIFIER column is used by the user to enter a
27 unique identifier made up of symbols, alpha or number characters
28 or both by which the program data stream is to be known by the
29 user, for example SPORTS for Data Stream 1, HOBBIES for Data
30 Stream 2, etc. Such capabilities are described in considerable
31 detail by Beery in U.S. Patent 5,068,734, which prior art patent
32 is incorporated herein by reference. The characters, symbols and

1 other information for entry in the spread sheet may be selected
2 from a list at the bottom of the spread sheet display by use of
3 the programmable keys A-D which are programmed and labeled to act
4 as cursor movement keys.

5 The function key F1 is configured to act as a select
6 key to first select the spread sheet location into which
7 information is being programmed and then select the character,
8 symbol, etc. on which the cursor is placed. Information so
9 entered via the User Remote is transmitted to the Data Manager
10 which records and stores the information and uses it to
11 facilitate User selection of programs to be watched as described
12 by Beery.

13 The PROGRAM STORAGE TIME 1 column is used to enter a
14 range of times during which a storage priority is to be assigned
15 to the corresponding program data stream. For example, if the
16 User wishes to record a sports highlights show which is
17 transmitted from 6:00 to 7:00 PM Monday thru Friday, this
18 information is entered via cursor movement as previously de-
19 scribed.

20 The STORAGE TIME 1 PRIORITY is a numerical priority
21 which is used to determine what programs are overwritten in the
22 event of insufficient memory. The lower the priority number the
23 more desired the storage of the program. Thus if it is desired to
24 store two programs at the same time, and memory is only available
25 for one, the higher priority (lower number) program is stored.
26 In addition, if insufficient memory is available and there is a
27 lower priority program already stored in memory the higher
28 priority program will overwrite it. The STORE PERIOD lets the
29 User assign a length of time the program is stored before it may
30 be overwritten by a lower priority program.

31 The MOST/LEAST RECENT OVERWRITE lets the User choose to
32 have the incoming program overwrite the most recent or least

1 recent stored version of the same program if there is no memory
2 available to store an incoming program because of relatively low
3 priority as compared to what is stored in memory.

4 A second set of storage parameters is also preferably
5 provided in order to allow more storage selections. If desired,
6 even more storage parameter sets may be provided. After filling
7 in the desired information, a typical spread sheet might look as
8 shown in Figure 5. Note that there are two #2 priorities in these
9 entries. This is acceptable because they take place at different
10 times. In the event the User attempts to enter conflicting
11 information which the Data Manager would be unable to
12 accommodate, a warning is preferably provided, such as by causing
13 a short beep to be emitted from the audio transducer and flashing
14 the conflicting entries. After finishing the entries of
15 information in the spread sheet, the user exits that feature.

16 The F3 key shown also provides access to a listing of
17 all currently stored programs in memory which the User may use to
18 play back a stored program. The user will simply highlight the
19 stored program he wishes to view with the cursor arrow keys
20 (programmed key A-D) and again presses the F3 key. An exit option
21 is provided and may be highlighted by the cursor with the F3 Key
22 to exit. The F3 key further provides access to system default
23 conditions. These defaults include the following: Allow
24 overwrite of program after viewing entire program and allow
25 overwrite of program minutes after viewing etc. These functions
26 also determine how long to wait before a viewed program is
27 discarded. For example it may be desired to retain educational
28 programs, but to immediately discard entertainment programs. It
29 further may be desired to allow access to specific programs or
30 types by password. This prevents unauthorized persons from
31 viewing identified programs. Playback speed is also setable.
32 This feature allows stored programs to be played back faster (or

1 slower) than normal, thus coupling the information or
2 entertainment delivery to the viewers ability to receive and
3 process. One can also select program types for storage and/or
4 preferred viewing programs and program types. These are a user
5 convenience features. Configuration to interface with other
6 services allows the hardware to match the particular set of
7 services the user desires. The Auto Store Buffer reserves time
8 and overwrite priority. This allows a User to pause a program
9 being received from the Program Data Stream with the invention
10 operating to continue storing the received data so that when the
11 User returns to viewing and disables the pause the User begins
12 where he stopped without loss of program material. The buffer
13 reserve time determines how much memory is reserved for this
14 storage function and consequently how long the User may keep the
15 system in pause and be guaranteed of no loss of program. The
16 Auto Store Buffer catch up rate allows a user to return to
17 viewing a program being received from the Program Data Stream
18 after a pause, while insuring he will be viewing the stored
19 portion of the program from the Auto Store Buffer. It is
20 desirable to read this information out of the buffer at faster
21 than normal rate. In this fashion, the program is read out of the
22 buffer faster than the program being written into the buffer and
23 consequently the buffer length will be continually shortened to
24 zero. This feature both returns the User to real time viewing,
25 thus allowing him to finish viewing the program when it actually
26 ends so he can go on to watch another Program Data Stream program
27 when it starts, and returns the Auto Store Buffer to an empty
28 state in preparation for pausing at another interruption. It
29 might be noted that when the stored portion of the program from
30 the Auto Store Buffer is read out of the buffer at faster than
31 normal rate, or when stored programs are read out at faster or
32 slower than the normal rate, that an audio pitch shift and video

1 motion artifact would normally occur. It is preferred to correct
2 these artifacts by use of the invention described in copending
3 U.S. Patent Application serial number 322,069 [incorporated
4 herein by reference].

5 The present invention includes a conversion system as
6 set forth in 322,069 and devices that incorporate it, which
7 conversion system can convert an input signal having frequency
8 related information normally sustained over a first length of
9 time into an output signal having substantially the same
10 perceived frequency related information, with the information now
11 normally sustained over a second length of time alternately just
12 frequency, and/or frequency and length of time can be modified.
13 The theory behind this operation is shown in the FIGURES,
14 including FIGURE 7. The theory behind the invention involves
15 getting an input signal 10 (Block I). This signal has frequency
16 based information sustained over a period of time. This input
17 signal 10 is provided to a signal modification circuit 50 (Block
18 II). The signal modification circuit 50 adds or subtracts
19 samples 15 to or from the input signal 10 according to certain
20 principles, mathematical principles normally based primarily on
21 the ratio of frequency and/or time between the input 10 and
22 output 100 signals and the complexity of the signals. The signal
23 modification circuit 50 then remits an output signal 100 (Block
24 III), which output signal 100 has a relationship to the input
25 signal 10 as set by the certain mathematical principles. One
26 skilled in the art should recognize that the devices disclosed in
27 this application could alter frequency over the same length of
28 time, alter frequency and length of time, and otherwise function.
29 The easiest way to do this would be by altering sample and/or
30 clock rates. For uniformity, this application will primarily
31 utilize as an example devices producing an output signal that
32 perceptibly has the same frequency related information as the

1 input signal 10 and may also be sustained over a different length
2 of time.

3 In this operation, both the input 10 and output 100
4 signals have frequency related information on them. The output
5 100 signal can be either expanded or compressed relative to the
6 input signal 10. The signals themselves can be audio,
7 television, computer signals, or other signals having frequency
8 related information thereon. Further, the devices can be used in
9 singular form (for example a television video signal), paired
10 form (for example right and left stereo audio signals), or in
11 other combinations including synchronizing the output signal to a
12 related signal (for example synchronizing audio to video). The
13 signals themselves can be in analog or digital form. A digital
14 form is presently preferred in that technology is presently more
15 established for digital processing of complex wave forms.
16 However, with the increasing advances in analog circuitry
17 including the use of charged coupled devices (CCD's), it is
18 envisioned that soon analog processors may be able to process the
19 complex signals as well and perhaps better.

20 The digital signals may be coded in pulse code
21 modulation (PCM), pulse width modulation (PWM), pulse length
22 modulation (PLM), pulse density modulation (PDM), pulse amplitude
23 modulation (PAM), pulse position modulation (PPM), pulse number
24 modulation (PNM), pulse frequency modulation (PFM), pulse
25 interval modulation (PIM), or other coding scheme. Pulse
26 amplitude modulation will be utilized in the explanation of the
27 invention. The location of the signal modification circuit 50 in
28 the overall replication path is not critical. In most instances,
29 the signal modification circuit 50 would be located after some
30 sort of signal storage means for modification of the stored
31 signal. This is generally preferred in that the stored signal
32 would contain the highest quality signal. Such stored signal

1 could also be otherwise used. However, the signal modification
2 circuit 50 could be located prior to the storage means or even
3 within such storage means. The circuit 50 could also operate in
4 real time. Further, the order of the conversion steps are not
5 critical as long as all steps are accomplished. For example, the
6 clocking shift and analog to digital conversion could occur prior
7 to real time signal modification in the overall frequency
8 conversion of an analog signal. An example of this would be
9 playing an answering machine at high speeds with subsequent real
10 time frequency conversion to lower the voice pitch to normal
11 values.

12 Further example in FIGURE 7 the storage means could be
13 located before/after or between any of the blocks of circuitry at
14 points A-H respectively. The operation of the invention is thus
15 also not dependent on a storage location. FIGURE 8 is a block
16 diagram of the signal modification circuit 50 receiving an input
17 signal 10 sustained over a first length of time 13 at a first
18 ascertainable frequency. In real time this length of time 13
19 would be the period of production of the input signal 10. As the
20 signal 10 utilized as a uniform example in this specification is
21 an analog signal, a digital converter 14 converts the input
22 analog signal 10 into a digitally sampled version 20 of the input
23 analog signal 10 (if the input signal 10 was itself digital or
24 already a digitally sampled version of an analog signal, no
25 conversion would normally be necessary; oversampling however,
26 might be appropriate. The inclusion of the converter 14 in the
27 modification circuit 50 is thus dependent on the nature of the
28 processed signals). In the particular circuitry example of the
29 figures, the input signal 10 is an analog signal having an alpha
30 length 13. Here, applicant defines alpha length as the time
31 duration of a contiguous signal block, exclusive of any reset
32 operations (reset operations will be addressed in detail below).

1 This input signal 10 is normally replicated over a certain time
2 period, a period normally directly related to the alpha length.
3 The input signal 10 normally exists for reproduction over a
4 certain set length of time, a time length analogous to inverse
5 clock rate including real time. In FIGURES 8 and 22, input clock
6 refers to the speed of production or reproduction of the input
7 signal. The input sample rate refers to the rate at which
8 discrete time samples are presented to the signal modification
9 circuit. The input clock and input sample rate may or may not be
10 related. For example, if the input source is an analog tape
11 player, the input clock would refer to the speed of the tape.
12 Tape speed might be variable, while the input sample rate may or
13 may not be variable. As another example, the input source may be
14 a compact disk player outputting digital samples at a 44.1kHz
15 rate. In this case, no continuous time to discrete time
16 conversion is necessary. If no sample rate conversion was used,
17 the input sample rate would here be the same as the input clock
18 rate. If the speed of playback of the compact disk was varied,
19 then both the input clock and input sample rate would vary. The
20 output sample rate is the rate at which discrete time samples are
21 output from the signal modification circuit. It may or may not
22 be equal to the input sample rate. The output clock rate refers
23 to the speed of production of the output signal, and may or may
24 not be related to the output sample rate. The input signal 10 is
25 normally preferably fed into a digital converter 14 in order to
26 replicate such input signal 10 in digital samples 15. The nature
27 and rate of the digital sampling is selected in accord with the
28 overall circuitry design. Examples of the type of digital
29 sampling that can be utilized have been previously set forth.
30 For uniformity, the preferred embodiment of the invention will be
31 set forth with pulse amplitude modulation (PAM) digital sampling.
32 It is preferred that the digital coding and/or rate be

1 selected in respect to the nature and frequencies of both the
2 input and output signals. For example, according to the sampling
3 theory, a sampling rate of a little over twice the highest
4 expected frequency will allow for the accurate reproduction of an
5 analog signal with minimal distortion. An example of this is the
6 44.1 kHz sampling rate for common compact disks. In addition to
7 this, the sampling rate must be selected in order to provide for
8 the compression/expansion of the signal in an accurate manner.
9 This entails a review of the signal content. In specific, if a
10 computer on/off binary signal was involved with a conversion of
11 3:2, a sampling rate three times the clock speed of the input
12 signal would provide for completely accurate conversion (fig 11).
13 However, with an audio signal at the same somewhat extreme
14 example 3:2 reduction, a sampling rate of twice the frequency of
15 the input audio signal (for example a sampling rate of 44.1 kHz)
16 would provide a normally unacceptable result due to the
17 distortion on the output signal 100. The reason for this would
18 be that aliasing would occur if one third (1/3) the samples were
19 removed. It is therefore necessary to sample the audio input
20 signal 10 at a rate much higher than the Nyquist rate in order to
21 provide for an acceptable output signal for the analog signal
22 (fig 17). Over and above this restriction, it is preferred that
23 any input signal 10 be sampled at as high a rate as possible, in
24 order that the addition/deletion of individual samples would have
25 a minimal effect on the information available on such input
26 signal 10. For example, the deletion of one out of every ten
27 samples at a 10,000 times over sampling rate would have less
28 artifacts than the deletion of one out of ten samples at a ten
29 times oversampling rate although both provide the same 10 percent
30 (10%) signal compression. The reason for this is that with
31 higher rate sampling, the many artifacts which would be produced
32 would occur at an extremely high frequency, with many occurring

1 at a frequency above that perceptible to the senses of the
2 consumer. The Philip's pulse amplitude modulation at a standard
3 rate of 256 over sampling (256x44.1 kHz) is a natural sampling
4 technique for the invention in audio applications.

5 The difference ratio 51 that is input to the actual
6 modification circuit 52 determines the scope and nature of the
7 relationship between the input 10 and output 100 signals. The
8 general concept is that there is an input signal 10 which has
9 frequency related information, which input signal 10 further has
10 some frequency and/or time ratio to the output signal 100,
11 normally a ratio based on the times of expected signal
12 production. If time is the determinant, the difference ratio is
13 selected such that the output signal 100 when perceived has the
14 same frequency related content as the input signal 10.
15 Alternately the output signal 100 may have the same time as the
16 input, but a different frequency or both may be varied
17 simultaneously.

18 The difference ratio may be defined as the output
19 frequency time product, divided by the input frequency time
20 product. For example, suppose that the difference ratio is
21 0.855. If the input and output times are the same, then the
22 output frequency is 0.855 the input frequency. If the input and
23 output frequencies are the same, then the output time is 0.855
24 the input time. If the output frequency is 0.95 the input
25 frequency, then the output time would be 0.9 the input time,
26 since 0.95 multiplied by 0.9 equals 0.855.

27 The difference ratio 51 can be set manually or
28 automatically. An example of the former would be having a
29 technician dial in a factor representative of the input length
30 and then a second factor representative of the output length.
31 This type of manual setting would be particularly appropriate
32 where the technician knew that a thirty (30) minute television

1 program needed to be inserted into a twenty eight (28) minute
2 time slot. As an example of the automatic setting, in television
3 signals the horizontal sync pulses could be utilized to
4 automatically decompress a tape recorded television movie. This
5 type of automatic functioning would be particularly appropriate
6 for signals having known, repetitive, determinable attributes or
7 where the function of the circuitry can be readily determined
8 (for example a profanity dump) and/or a known real time length
9 and known time for actual presentation.

10 In the circuitry of FIGURES 8 and 22, the difference
11 ratio is as previously defined. This ratio has been previously
12 determined. Pitch shift may be obtained by sample insertion or
13 deletion, if the input and output sample rates are the same.
14 Alternatively, pitch shift may be obtained by using differing
15 input and output sample rates, without sample insertion or
16 deletion. Additionally, a combination of sample
17 insertion/deletion and differing sample rates may be used. The
18 sample rates preferably are at least greater than the Nyquist
19 rate for both input and output. Over and above this, distortion
20 considerations could require that the input signal be sampled at
21 a rate much higher (for example 20 times) the highest input
22 frequency in order to insure production of the output signal with
23 minimal distortion. Note, however, that in noncritical
24 applications the sampling rates can be much lower, particularly
25 if the signals can be ~~bandwidth~~ limited while retaining
26 acceptable information content (an example of this would be ~~band-~~
27 ~~bandwidth~~ width limiting an audio signal to 5kHz).

28 As shown in FIGURES 9-23, the modification circuit 52
29 selects at least one sample 22 from the digital sampled version
30 20 of the input signal 10 and generates a second plurality of
31 digital samples 120 by altering the number of the digital sampled
32 version 20 of the input signal 10 by the selected digital

1 sample(s) 22. This can be by addition to expand (samples 122 in
2 figs 12 and 13) or by subtraction to compress (samples 27 in fig
3 19) as appropriate. The location of the added/deleted samples is
4 selected in view of the signal content so as to minimize
5 artifacts. For very high oversampling rates, the samples can be
6 spread out over the entire alpha length of the signal. For lower
7 oversampling rates, locations of least slope, least differences,
8 signal peaks, or other minimal signal information points are
9 preferred.

10 Note that figures 9-21 are given by way of example.
11 Other sampling/modification methods could also be utilized with
12 the invention. Note also that for clarity of explanation in
13 these figures that the input sample is converted to digital by a
14 leading edge sample and hold circuit (left edge), while the
15 output sample is converted to analog by a trailing edge
16 conversion circuit (right edge). Alternate conversion circuits
17 could be utilized if desired. For ease of comprehension, no
18 interpolation is used in figures 9-21.

19 The second plurality of digital samples 120 can be
20 interpolated to reduce distortion caused by replication or
21 deletion of the selected digital sample 22 if appropriate. A
22 second digital converter 114 then generates an output signal 100
23 from the second plurality of digital samples 120 over the second
24 duration of time 113 (again the inclusion of this convertor is
25 dependent on the nature of the output signal). In the example
26 shown, this produces a signal having substantially the same first
27 frequency when clocked or reproduced at the new speed provided
28 that the rate of occurrence of altered samples 22 relative to the
29 input sample rate corresponds to the ratio between the first 13
30 and second 113 duration times. Compare the analog input signal
31 10 of FIGURE 9 with the output analog signal 100 of FIGURE 16,
32 which output signal 100 is being produced during a different,

1 shorter, length of time: In real time 80, the perceived
2 frequencies or alpha length of the signals are the same. In this
3 respect, it is noted that minor unobjectionable shifts could be
4 accepted by the overseeing technician, this even though the pitch
5 of the resultant signal is not absolutely accurate. Alternately
6 the output may have a different frequency and same duration or a
7 combination of different frequency and duration.

8 It should again be appreciated by those skilled in the
9 art that either the digital converter 14 or the digital converter
10 114 may be optional in the event that either the input signal 10
11 or the output signal 100 is a digital signal of suitable signal
12 content to allow for acceptable modification. Otherwise,
13 oversampling would normally be appropriate.

14 The selected digital sample(s) 22 is added (fig 11) to
15 the sampled version 20 of the input signal 10 to provide pitch
16 correction to facilitate the prior or subsequent decrease of the
17 duration time. The selected digital sample(s) 22 is removed (fig
18 19) from the sampled version 20 of the input signal 10 to provide
19 pitch correction to facilitate the prior or subsequent increase
20 of the duration time. This will be discussed more extensively
21 later, especially with respect to FIGURES 22-24.

22 The signal modification circuit 50 adds or subtracts to
23 the apparent alpha length of the input signal 10 according to the
24 difference ratio in order to produce the output signal 100.

25 With present digital technology, this signal
26 modification circuit 50 would begin with digital signals or a
27 digital sampling replication 15 of an analog signal. This signal
28 modification circuit 50 then repeats (to add or expand) or
29 deletes (to subtract or compress) from these samples in order to
30 alter the input signal 10 to an output signal 100 in accord with
31 the set difference ratio. (Note again that a digital signal
32 might, like an analog signal, have to be digitally over sampled

1 to achieve acceptable distortion performance.)

2 A more sophisticated signal modification circuit 50
3 could average or linearly or otherwise interpolate the modified
4 samples in order to optimize the functioning of the device in
5 certain applications.

6 For example, a theoretical analysis of the spectrum
7 resulting from applying a 5.6 percent expansion to a sine wave
8 was performed. The sine wave period was 36 samples. The purpose
9 of the analysis was to determine the relative distortion levels
10 resulting from the insertion of samples at different phases of
11 the input sine wave. Two samples per period were inserted. The
12 type of linear interpolation used in the preferred embodiment is
13 essentially the second order approximation method used for sample
14 rate conversion. Proakis, John G., Rader, Charles M., Ling,
15 Fuyun, and Nikias, Chrysostomos L., Advanced Digital Signal
16 Processing, Macmillen, 1992. This particular interpolation
17 operates along the entire signal, and weighs two adjacent samples
18 in proportion to the distance from the last sample insertion.
19 This type of interpolation gives exact (within quantification
20 limits) output in the case of a linear ramp signal with constant
21 slope (zero second difference). Three insertion points were
22 examined: peaks, zero crossing, and ~~30°~~ lagging from zero
23 crossing. Insertion of samples at the zero crossing resulted in
24 the lowest distortion of the three. Insertion of samples at the
25 peaks was slightly inferior to the zero crossing. Insertion of
26 samples at the ~~30°~~ points resulted in the highest distortion. A
27 feature of the zero crossing point of a sine wave is that it is
28 the location of minimum second difference magnitude. A feature
29 of the positive and negative peaks of a sine wave is that they
30 are the location of minimum slope, or minimum first difference,
31 magnitude. A feature of points on the sine wave which are
32 removed from the peaks or zero crossings, such as the ~~30°~~ phase

1 point, is that neither the first or second difference is
2 minimized.

3 Sample insertion at the peaks and at the zero crossings
4 was also investigated for the case of no interpolation. In this
5 case, insertion at the peaks gave lower distortion. Distortion
6 performance in both cases was significantly worse than that
7 obtained where interpolation was used.

8 It is envisioned that other interpolation algorithms
9 may be advantageous from a performance standpoint. Examples of
10 other algorithms would be polyphase subfiltering, higher order
11 Lagrange polynomial interpolation, and finite impulse response
12 low-pass filtering. In the case of expansion, it may also be
13 advantageous for the added sample to be of some value other than
14 the value of the immediately preceding sample.

15 Customarily, the signal modification circuit 50 would
16 contain a delay length preferably of the variable type, the
17 length of which must at least allow for the appropriate shifting
18 of the signals to add or subtract whole cycles. Specifically,
19 the maximum shift between the input signal 10 and the output
20 signal 100 should be within the effective delay length of the
21 available memory. Further, to provide for a smooth output signal
22 100, the present invention preferably uses a memory delay longer
23 than this period in order to provide for a seamless operation.

24 The present invention accomplishes this with less than
25 the amount of memory otherwise needed by comparing a first and
26 second signal in order to reset the information in the memory (as
27 later described) to add or delete blocks or cycles thus to
28 provide for a seamless integration of the signals. In general,
29 the more memory that is available, the more time can pass before
30 the device is reset subject to an ascertainable artifact
31 override. For complex audio signals, up to a point, the quicker
32 the resetting; normally the less ascertainable the artifacts as

1 will be described in more detail below. In addition, an even
2 greater memory would allow an operator to delete or add blocks,
3 cycles, or multiple cycles of signal information with no pitch
4 change.

5 The delay could be a single memory if variable taps
6 were available and the signal was actively followed through such
7 variable taps by the signal modification circuit 50. Changing
8 over between effectively two separate memory delay lengths 56, 57
9 is preferred, which delay lengths are each long enough to provide
10 for the later described resetting, because of the way the design
11 evolved. A single memory delay element was originally used.
12 Later, a second memory delay element was added, since this was,
13 at the time, the easiest way to accommodate the needed later
14 described cross fade reset operation. At any given time,
15 exclusive of reset operations, one memory circuit would be
16 actively utilized in real time by the signal modification
17 circuit, while the other memory preferably would continue to be
18 updated with input signal data. An example of this is the two
19 stretch cell embodiments set forth in FIGURES 26 and 27.

20 The circuitry of FIGURES 23 and 27-28 include two
21 effective memory lines 56 and 57 together with two modification
22 circuits 60 and 61. FIGURE 23 utilizes two separate RAM memories
23 while FIGURES 26 and 27 utilize a single RAM memory, with two
24 different address spaces allocated respectively to two stretch
25 cells to allow resetting.

26 The memory lines 56, 57 are preferably RAM memory
27 circuits. These circuits provide for a delay necessary for the
28 processing to occur. The length of these memory circuits is
29 chosen in order to optimize the performance of the overall
30 circuitry while at the same time preferably minimizing expense.
31 The selection of length is normally a compromise between
32 excessive delay versus the ascertainable artifacts which might

1 occur during resetting at an earlier than appropriate time or
2 resetting at too high a rate. In general, changing over more
3 quickly reduces information loss. However, changing over too
4 quickly results in unacceptable artifacts, so a compromise is
5 chosen. Also, in general, optimization of performance is
6 determinative of the preferable length for the memories 56, 57,
7 even though theoretically an infinite memory length could be
8 used. (Too long a delay can produce noticeable gap and/or echo
9 effects. It also violates EIA/TIA-250-C.) Due to the use of two
10 memory lines, and the changing therebetween (as later described),
11 memory lengths of from 38 mS to 149 mS are more than sufficient
12 for a normal audio signal. This memory is sufficiently long to
13 allow for the smooth crossover between memories 56, 57 while at
14 the same time storing sufficient samples so as to support the
15 typically experienced maximum time between crossovers. Note that
16 the length of the memory is a design choice. For example, there
17 are frequent times of audio silence in a television talk show.
18 If the memory was sufficiently long as a function of the expected
19 length between silences in audio content, and the duration of the
20 silence was at least as long as the section of memory to be
21 traversed by the reset, the memory could be reset during these
22 times of silence, thus not dumping or repeating any audio
23 information. The length of memory required is the expected
24 length between silences multiplied by the conversion factor. For
25 example, for 0.4 seconds between silences at ten percent
26 expansion or compression, 40 mS of memory is typically required.
27 Further example in a symphony orchestra a memory technically long
28 enough to work may produce artifacts due to too frequent resets.
29 A longer memory accompanied by a reset prevention control would
30 therefore be used, preferably delaying resetting to a time of
31 silence or otherwise when least artifacts would occur. An
32 additional example would be with television video content wherein

1 there are frequent times of static images and/or screen changes.
2 These can be located with a motion detector. By adding or
3 deleting frames thus changing over video during these times,
4 video artifacts are reduced to a minimum. Further, if the
5 signals of any nature are compressed or expanded prior to signal
6 modification and the sampling rate is high enough, and acceptable
7 reset opportunities occur with sufficient frequency, conversion
8 can occur with low average throughput delay. It is, therefore,
9 important to recognize that the invention can be optimized for a
10 given signal by slightly altering its specific implementation.

11 The modification circuits 60, 61 add or subtract
12 samples to the signals contained within the memories 56, 57,
13 respectively. This modification of the samples can occur while
14 the samples are being fed into the memories 56, 57, while they
15 are being removed from the memories, or otherwise.

16 As previously described, the rate of digital sampling
17 is normally dependent on the complexity and frequency of the
18 signals. In general, the more complex the signal and/or the more
19 this conversion ratio is removed from unity, the more samples
20 will be needed. The reason for this is that using too few
21 samples in a complex, high frequency conversion will result in
22 excessive distortion. For example with a 30MHz computer square
23 wave high/low input signal, three samples per clock period would
24 be sufficient to slow the signal down to 20MHz (see fig 16).
25 However, with a 20kHz audio signal, a sample rate much higher
26 relative to signal frequency would be necessary to provide a 5
27 percent expansion without audible artifacts (see representative
28 fig 17). This is because the information content of the computer
29 signal is accurately conveyed solely by the on/off state. Thus
30 the digital sampling rate must be carefully selected in view of
31 the signals, both input 10 and output 100, as well as the
32 difference ratio 51 to be encountered.

1 Changing over between the signal of the first memory 56
2 and the signal of the second memory 57 is accomplished by a reset
3 control 65. When the reset control 65 operates, the signal
4 modification circuit 50 changes over to the previously inactive
5 memory circuit to remit the output signal 100. The other once
6 active memory at the same time becomes disconnected from the
7 output. The result is to increase or decrease the effective
8 length of the overall memory.

9 Note, if samples are taken out of the memory more
10 slowly than they are put in, the delay length will slowly
11 increase to maximum. At maximum delay, there will be no
12 available memory for the next sample to be put into. Conversely,
13 if samples are taken out faster than put in, the delay will
14 shorten to nothing. At zero delay, there will be no stored
15 sample to be taken out. It thus is desired to reset the memories
16 before they are full or empty respectively, and preferably so
17 that whole cycles of signal are added or deleted. By resetting
18 or changing over memories, a portion of the signal will be
19 repeated, preferably an integral signal, or a portion of the
20 signal will be lost, again preferably an integral cycle. The net
21 gain in either case, however, is to vastly increase the amount of
22 apparent memory.

23 The reset control 65 operates by comparing two signals
24 in order to determine their similarity, with the changing over
25 between the signals in memory occurring based on this similarity.
26 The purpose of the reset control 65 is to maintain the overall
27 throughput delay within acceptable limits. The signals being
28 compared typically should include a delayed signal and another
29 signal, which may itself be also delayed or not. For example, in
30 a compression circuit, samples are being removed and a signal is
31 effectively output from memory faster than it is being input.
32 For this reason, the reset point could be at maximum delay or at

1 the end of the memory. A delayed signal at this point is then
2 compared to the relatively undelayed signal that is being used by
3 the modification circuit for changeover to maximum delay.
4 However, in an expansion circuit, samples are being added and a
5 signal is effectively output from memory more slowly than it is
6 being input. For this reason, the reset point could be at
7 minimum delay, or at the beginning of the memory. A relatively
8 undelayed signal at this point (which could even be the input
9 signal) is then compared to a relatively delayed signal that is
10 being used by the modification circuit for changeover to minimum
11 delay. As an additional example, the reset control 65 could be a
12 computer that has as a signal feed of only the input signal,
13 which the computer compares with time shifted versions of such
14 signal to operate this reset control 65 through analytical
15 analysis, essentially comparing two versions of the single input
16 signal for similarity; this with no other direct connection to
17 any signal modification circuit signal input or output. As a
18 further example, the reset control could be a computer that
19 compares a plurality of signals over a range at one end of a
20 memory with a second plurality of signals over a range at the
21 other end of a memory, with the reset occurring between the two
22 most similar signals. In this device, the signals being compared
23 would be developed from an analysis of a plurality of signals.
24 While the resulting reset might not produce the maximum amount of
25 available memory (i.e., be to the end of the memory), complex
26 signals would be effectively processed. Therefore, depending on
27 circuit design, the signals compared for similarity may vary from
28 that disclosed herein. The key is that the signals have a
29 statistical probability of being similar and are representative
30 of signals displaced from each other in the memory. For example,
31 the reset control could compare: a) the signal at the output of
32 one memory 56, 57 to the input of the other memory 56, 57; b) the

1 output 100 to the input 10; or, c) otherwise as desired or
2 appropriate. In the preferred expansion embodiment of this
3 specification, the input signal and output from the active memory
4 are compared. In the preferred compression embodiment, the
5 output from the active memory and the signal delayed relative to
6 this output are compared.

7 The reset control 65 in ascertaining similarity,
8 preferably, compares the signals for: a) relative slope between
9 signals; and, b) relative amplitude between signals. These are
10 compared to preset thresholds. Signals meeting the criteria of
11 low relative slope and amplitude include periods of no
12 information (i.e., silence in audio). Video signals could be
13 compared for scene change points for the addition/deletion of
14 frames in a video image in an alternative embodiment. Video
15 signals could also be compared for static video images, in an
16 alternative embodiment.

17 The Algorithms used to extract signal comparison
18 information must be selected consistent with the type of coding
19 used. It is preferred that the compared signals be
20 examined for similarity in as many characteristics as practical.
21 For example, the use of zero crossover in a similar direction
22 alone in a reset control could produce an artifact if one signal
23 was a high frequency signal at that point while the other was a
24 low frequency signal. Similarly, least relative slope alone
25 could cause unacceptable artifacts to critical listeners of an
26 orchestra if resetting occurs more rapidly than is absolutely
27 necessary. Look forward and look back comparisons would thus
28 preferably be utilized in the reset control 65 so as to optimize
29 the overall comparison with time displaced information as well as
30 current signal status. Further, the reset control 65 would
31 preferably include an override in response to these overall
32 comparisons in order to limit unneeded resets, thus optimizing

1 the comparison procedure. In general, the more comparison
2 attributes are included, the better the operation of the reset
3 control 65.

4 The reset function is often accompanied by a repeat of
5 signal (pitch increase mode; samples removed) or discard of
6 signal (pitch decrease mode; samples added).

7 Using an example memory device that is capable of both
8 modes (fig 31) with two parallel memory lines 56, 57 and two
9 signal modification circuits 60, 61, the reason for this signal
10 repeat/deletion can be readily understood. In this device, an
11 input signal 10 is being continually fed into the beginning of
12 two RAM memory lines 56, 57.

13 In the pitch increase mode A, the active signal
14 modification circuit (60 shown) uses signal data at a somewhat
15 faster rate than it is being fed into the memory line 56 (the
16 actual rate dependent on the expansion ratio). This causes the
17 active signal modification circuit 60 to relatively advance up
18 the memory line 56. While this is occurring, the reset control
19 65 is examining two signals for similarity. In the embodiment
20 shown, the signal being output by the active signal modification
21 circuit 60 and the signal at the circuits reset position are
22 compared (as depicted by dotted lines in all figures). When the
23 signals are similar (or when the active memory line 56 is used
24 up), a reset occurs. This causes the other memory line 57 to
25 return to the relative reset point and other modification circuit
26 61 to become active. However, since the input signal 10 has been
27 continually fed into both memory lines 56, 57, this reset causes
28 a certain portion 58 of the input signal 10 to be processed for a
29 second time repeating this data at the output of the signal
30 modification circuit 50. As the input signal 10 is periodic, and
31 an integral number of signal periods is repeated, the artifact is
32 acceptable. For example, as shown in the FIGURES 23-25, the

1 actual repeat would normally be one or more complete cycle of the
2 input signal. The actual reset would repeat only a fraction of
3 the actual signal content. In fact, this fraction is typically
4 equal to the compression factor.

5 In the pitch decrease mode B, the active signal
6 modification circuit (60 shown) uses signal data at a slower rate
7 than it is being fed into the memory line 56. This causes the
8 active signal modification circuit 60 to relatively retreat down
9 the memory line 56. While this is occurring, again the reset
10 control 65 is examining two signals for similarity. In the
11 embodiment shown; the signal being utilized by the active signal
12 modification circuit 60 and the signal at the circuits reset or
13 input position (dotted lines in all figures) are compared. When
14 the signals are similar (or when the active memory line 56 is
15 used up), a reset occurs. This causes the other memory line 57
16 and other modification circuit 61 to become active. However,
17 since the input signal 10 has been continually fed into both
18 memory lines 56, 57, the reset causes a certain portion 59 of the
19 input signal 10 to be never processed, thus deleting this data
20 from the output of the signal modification circuit 50. Again, as
21 the input signal is Periodic, and an integral number of periods
22 is deleted, the artifact is acceptable, especially given the ways
23 described herein of reducing its noticeability.

24 Note this example uses two memory lines 56, 57 and two
25 modification circuits 60, 61 with a single sample rate for
26 clarity of explanation. In other embodiments, the memory lines
27 56, 57 could be combined, a single modification circuit could be
28 utilized, only increase or decrease, or both increase and
29 decrease, could be provided in a single circuit, the processing
30 could occur in real time for pitch shifting and other signals
31 could be compared for reset control. Further, the signals in
32 memory could be clocked out at higher or slower rates than being

1 input, thus providing the alteration of the alpha length of the
2 input signal without movement of the signals to the modification
3 circuits (which in both compress and contract could be located at
4 the end of two individually differing clocked memory lines).
5 Examples of these and other embodiments are given here and
6 elsewhere in this application.

7 The resetting increases or decreases the effective
8 length of the overall memory with acceptable artifacts by
9 changing over between effective memories as previously described.

10 In the preferred embodiment, when the chosen
11 parameter(s) are similar, the reset control 65 changes over
12 between the relative memories 56, 57 as described. In addition,
13 the previously inactive memory 56, 57 is reset at the time of
14 changeover, thus extending its relative length.

15 Note that if there are multiple related channels, such
16 as stereo audio or surround sound, this switchover preferably
17 occurs when all important channels are similar at the same time,
18 thus minimizing perceived stereo or spatial phase shift. This
19 reduces the loss of stereo or spatial imaging. This correlation
20 is preferably occasioned by logically connecting each channel
21 associated reset control 66 to the reset control 65 for
22 cooperative signals in order to provide for comparisons of their
23 respective signals similarity.

24 In addition, in a possible alternative embodiment, if
25 the reset control 65 has not operated near to either end of an
26 operative total memory length, changing over is forced;
27 preferably based on some sort of optimization formula (ideally
28 computerized). This preferable forcing recognizes that a
29 particular memory length may run out of its ability to compensate
30 for the delay between the compared signals prior to the compared
31 signals being similar (as previously set forth), and thus might
32 produce annoying artifacts. Note also that if there are multiple

1 channels (for example again stereo audio), the signals might be
2 forced independently according to individual parameters. One
3 example of this would be if one channel had high frequency (such
4 as a fife), and the other channel had low frequency (such as
5 drums). The optimum forcing times for each respective channel
6 might not be coincidental. In this particular example, the low
7 channel might be forced at a different time from the high
8 channel: if the channels were forced simultaneously, there could
9 be high frequency cancellation and/or loss of imaging. It is
10 therefore appropriate for the forcing to be under the control of
11 some logic specifically designed for the nature of the signals.
12 For example with off/on computer signals, the two channels could
13 be forced independently: Each according to its own parameters.
14 However, for a stereo audio system or for an audio signal
15 synchronized with a video image, care must be taken not to
16 destroy the imaging and/or synchronization. The channels must
17 therefore be correlated to insure that this does not happen.

18 The circuitry in FIGURES 22 and 26-27 have a reset
19 control 65 which compares the intermediate signals in the
20 modification circuits 60, 61 for similarity with the reset
21 control 65 operating a cross fade control 70 to change over
22 between modification circuits 60, 61.

23 Note if the length of the delay in the memories 56, 57
24 was appropriately extended, the changing over could be
25 artificially manipulated including to allow for the deletion or
26 insertion of blocks of information while also reducing the
27 artifacts to a minimal amount. As an example of this, in talk/
28 show profanity memories, it would be possible to change over to
29 the inactive memory at the immediate end of the time of the
30 profanity, thus in effect resetting the profanity memory without
31 any additional loss of signal. As an additional example, a
32 documentary could add to or delete audio independently of the

1 video content by increasing or decreasing audio delay without
2 introducing an annoying pitch change. Further, if there is a
3 correlation between two signals, the use of the invention would
4 allow one to independently resync the signal's correlation
5 without introducing objectionable artifacts.

6 An example of how the input 10 and output 100 signals
7 may correlate will now be described in example form. In the
8 embodiment of the invention now specifically described, the input
9 10 and output 100 will be analog signals with frequency shifting
10 alone occurring.

11 The input signal 10 is a signal stored for production
12 over a first length of time. This input signal 10 has frequency
13 related information thereon. An example would be a television or
14 audio signal from a video cassette recorder or other storage
15 means. A simplified stylistic version of this input signal 10 is
16 shown in FIGURE 9 (in the actual signal, a more complex waveform
17 would normally occur; see FIGURE 12 for example). For reasons
18 not particularly important to this example, it is desired to
19 extend this example signal by substantially 5.6 percent without
20 altering the apparent frequency content thereon.

21 Note that figures 9-21 are given by way of example.
22 Other sampling/modification methods could also be utilized with
23 the invention. Note also that for clarity of explanation in
24 these figures that the input sample is converted to digital by a
25 leading edge sample and hold circuit (left edge), while the
26 output sample is converted to analog by a trailing edge
27 conversion circuit (right edge). Alternate conversion circuits
28 could be utilized if desired. For ease of comprehension, no
29 interpolation is used in figures 9-21.

30 The first step of this example is to replicate the
31 input signal 10 of FIGURE 9 into digital form. In the devices of
32 FIGURES 22 and 25 this is accomplished by a pulse amplitude

1 analog to digital converter 14. An example of this digital
2 sampled signal is shown in FIGURE 10. (Although pulse amplitude
3 modulation is shown for this digital example, it is to be
4 understood that other coding methods could be utilized without
5 deviating from the claimed invention. Examples include PWM, PEM,
6 PDM, PCM, PPM, PNM, PFM, PLM, and PIM.

7 In this FIGURE 10, the analog signal 10 has been
8 replicated into digital form 20 through the use of PAM,
9 specifically thirty six (36) digital samples 21, each having an
10 amplitude. In that the input signal 10 is to be compressed by
11 5.6 percent, this 5.6 percent is the equivalent of two samples of
12 our example digital wave 20 of FIGURE 5 (it is necessary then to
13 add two digital samples 22 to the input signal 10 in order to
14 frequency compensate such signal). This exemplifies the fact
15 that in the preferred embodiment the sampling rate preferably
16 must be high enough so as to allow the insertion (or deletion) of
17 a sample 21 in the replication of the output signal 100, without
18 introducing unacceptable distortion.

19 In general, the higher the sampling rate, the less
20 distortion will be introduced by the frequency conversion
21 process. This is particularly true in respect to the frequencies
22 where the consumer is most sensitive. In addition, it is
23 preferred that the samples 20 be inserted (or deleted) where any
24 artifacts would be least noticeable. In the case of a
25 significant expansion (or contraction), the samples would
26 preferably be spread out over the entire length of the wave form
27 (see fig 12 for a representative complex wave form).

28 Our example signal is a sine wave with the samples
29 added at the point of least slope; the peaks 23 of the positive
30 wave and negative wave, respectively. Therefore, needing only
31 two samples, at these two points the signal modification circuit
32 '50 inserts an additional sample 24 in both the positive and

1 negative series of digital samples 21. This produces the
2 modified digital signal 25 of FIGURE 12. A modified signal
3 without highlighting is shown in FIGURE 13, now representative of
4 the sampling 120 of the output signal 100. Note that FIGURE 7
5 has a peak sample repeated.

6 When the compressed digital representation of the
7 signal 120 in FIGURE 12 is taken through a digital to analog
8 converter 114, the result is the signal shown in FIGURE 14, an
9 output signal 100 having an effective alpha length 113 some 5.6
10 percent longer than the input signal 10 shown in FIGURE 4. The
11 difference between the two signals 10, 100 is shown in FIGURE 15.

12 Due to this difference, the output signal 100 can be
13 played back at a clock rate some 5.6 percent higher than the
14 input signal 10 in FIGURE 9 while at the same time producing a
15 signal having the same frequency content to the observer as
16 existed in the input signal 10. (Compare fig 9, i.e., the input
17 signal 10, with fig 16 wherein the output signal 100 is clocked
18 at a rate 5.6 percent higher than fig 9: The two signals produce
19 the same frequency content.) This would allow a television
20 station to shorten the time of a television program accordingly
21 without increasing the pitch of the related audio information.

22 It should be noted that in this example the
23 compression/expansion factor is equal to the inverse of the
24 number of samples between peaks. In the more general case, where
25 such a simple relationship did not exist between waveform period
26 and pitch shift factor, it typically would not necessarily be
27 possible to arbitrarily select the more favorable points for
28 sample insertion or deletion.

29 It should also be noted that in cases of types of
30 coding differing from the PAM of this example, differing sample
31 modification algorithms may be required.

32 The difference between our example input 10 and output

1 signal 100 is some 5.6 percent. However, any difference,
2 including this 5.6 percent, is cumulative for each cycle of the
3 input signal 10. For this reason, the memory necessary to
4 perform the function of modifying the input signal 10 into the
5 output signal 100 can be computed by multiplying the number of
6 repetitive cycles by the difference time factor, by 5.6 percent
7 in our example. This adds up very quickly to a significant
8 amount, an amount requiring ever increasing memory.

9 To avoid this, the applicant's invention uses the reset
10 control 65 to change over between effective memory points in the
11 signal modification circuit 50 so as to reuse the same effective
12 memory repeated times.

13 This reset control circuit 65 operates when the two
14 signals being compared are similar within prescribed parameters
15 as previously set forth. It then changes over between similar
16 signals. An example of the comparison can be seen in FIGURE 17.
17 This figure represents a circuit adding samples to a first analog
18 signal 63 to produce a second, expanded analog signal 64. In
19 this figure, after 38 cycles, the first analog signal 63 and the
20 second analog signal 64 both have a positive going similar slope,
21 same direction, zero crossings at the same location 70. If one
22 immediately reset the signals, and began the cycle anew at this
23 time, an individual to whom the signal 100 was addressed would
24 not notice any significant artifacts. For this reason, the
25 switchover could compensate for the increasing phase lag between
26 the signals with memory having a finite length. The cost of this
27 in FIGURE 23 is the loss of one cycle of the first analog signal
28 63, which one cycle would never be produced to be perceived by
29 the individual.

30 As previously set forth this resetting is most easily
31 accomplished by changing over between two memory lines 56, 57
32 accompanied by a resetting of the second memory line (as was

1 further described in respect to FIGURE 22). While this
2 compromises the input signal 10 information, this resetting
3 significantly reduces the amount of memory necessary for the
4 device to operate. More importantly, even if infinite memory
5 were available, resetting must still be done. Otherwise, the
6 desired effect of time compression or expansion would be
7 completely canceled. As an example of this, memory line 56 would
8 be utilized for the time 67 with memory line 57 utilized for the
9 time 68 to produce the output 64.

10 FIGURE 24 represents a circuit deleting samples of a
11 first analog signal 63 to produce a second compressed analog
12 signal 65. This figure is a graph comparing the first analog
13 signal 63 and the second analog signal 65 and illustrating the
14 reset 140 of the signals at a common amplitude, similar frequency
15 signal peak. At this time, again one would change over between
16 the two memory lines 56, 57 and simultaneously reset the second
17 memory line. This has the effect of adding to the output 100 by
18 repeating one cycle of the input signal 10 information, again a
19 resetting significantly reducing the amount of memory necessary
20 to operate unnoticeably as well as maintaining through delay
21 within acceptable limits. Again the two memory lines 56, 57
22 would preferably be utilized alternately to produce the output 64
23 without seams.

24 The invention finds particular application in MPEG
25 audio and video compression (figs 28-29). In the MPEG system,
26 there is a considerable amount of video processing which goes on
27 which is dependent upon the complexity of the video image which
28 is compressed and/or decompressed. This is also true for the
29 various audio signals which accompany the video. Due to the
30 differences in compression complexity, there is frequently a
31 corresponding variable delay interval in compression and/or
32 decompression time which causes missynchronization of the audio

1 and video signals when they are ultimately decompressed for use,
2 as for example by receipt of an MPEG compressed HDTV television
3 signal by a viewer.

4 In order to attempt to overcome the audio to video
5 asynchrony problem, the MPEG compression standard provides for
6 encoding a unique number in the compressed audio and video data
7 stream every 0.7 seconds or so at the time of compression. Upon
8 subsequent decompression, these numbers are presented to the
9 audio and video system decoders in order to facilitate a
10 comparison of the audio number to the video number in order to
11 allow the two to be brought back into relative synchrony at these
12 periodic times by manipulating the video via video frame
13 memories. This still, however, can produce ascertainable
14 artifacts tiring or objectionable to the observer. Further,
15 multiple frame video memory buffers are necessary to allow the
16 needed frame comparisons to repeat or drop identical frames.
17 This memory is expensive and the processing complex.

18 The above missynchronization of the audio and video
19 signals of a particular entertainment program can be a serious
20 problem, especially when the audio leads the video, as this is an
21 unnatural condition and leads to conscious or unconscious stress
22 in the viewer. This is an unfortunate byproduct of the MPEG
23 compression. The unnatural audio leading and/or trailing video
24 condition is also known to diminish the viewer's perception of
25 the quality, for example the entertainment value of the program
26 being viewed.

27 The present invention can be utilized to resynchronize
28 the signals, thus eliminating the tiring and objectionable
29 artifacts. Further, the multiple frame video delay and complex
30 comparisons of the MPEG standards are not needed even though
31 better synchronization is achieved. The invention accomplishes
32 this by effectively speeding up or slowing down the audio

1 signal(s) to synchronize it to the video, and does so without any
2 pitch change.

3 The invention preferably utilizes the automatic
4 reference signals to accomplish this synchronization. The two
5 preferred reference signals which are encoded at the time of MPEG
6 compression are SCR (System Clock Reference) and PTS
7 (Presentation Time Stamps), the details of which may be found in
8 the MPEG specification standards published by ISO/IEC. Other
9 compression standards suffer from the same problems and may make
10 use of these or similar SCR or PTS type schemes, which will be
11 referred to collectively here as time flags.

12 The encoded time flags thus represent the starting time
13 at which a particular video frame and its associated audio
14 signal(s) arrive at the encoder, and/or are to be played back
15 together from the decoder.

16 In this example MPEG system as it presently exists, if
17 the video decoder sees that the video frame it is about to play
18 back has a code which is later than that is, occurred after, the
19 audio which is currently being played back, a frame of the video
20 is repeated to bring the two close to synchrony. If the video
21 frame is before the audio which is currently being played back, a
22 frame is discarded. Such action, which is suggested by the MPEG
23 standard, finds only limited capability in preventing audio to
24 video asynchrony. Further, there are other problems with the
25 frame drop/frame repeat method of achieving synchronization.
26 First, adjustments may be made only in one frame increments,
27 giving rise to potential residual errors. Also, the required
28 video memory is costly compared to an equivalent amount of audio
29 memory. Further, it may be that it is needed to discard a frame
30 of video to synchronize signals, but the full frame might not yet
31 have arrived due to complex decoding requirements. More than one
32 frame of adjustment might also be needed, giving rise to the need

1 for even more video memory with the associated cost problems.
2 Since adjustment is made in frame jumps, this can also cause
3 motion related artifacts, and, if the relative delay is constant-
4 ly changing, the system can alternately repeat and delete frames
5 of video causing an artifact known as motion judder (jitter +
6 shudder). Further, the missynchronization that does exist could
7 cause subconscious or even conscious ascertainable artifacts,
8 reducing the viewer's enjoyment.

9 The invention of this application can be utilized in
10 conjunction with a continuously variable audio delay to provide a
11 better audio to video synchronization than in the present MPEG
12 frame drop/frame repeat standard. Further, this is achieved at a
13 lower cost. The invention preferably accomplishes this by adding
14 samples to the audio to allow the audio to be slowed down to re-
15 synchronize the signals (in the instance of advanced audio), or
16 deleting samples to allow the audio to be sped up to re-
17 synchronize the signals (in the instance of delayed audio). The
18 signal modification circuit may be used by itself or in
19 conjunction with a frame drop/frame repeat device.

20 The video signal to be output from the receiver's video
21 decoder precedes the audio. This delay allows the processing of
22 the video signal to synchronize the eventual audio signal output
23 with the video signal. (The resulting correspondingly advanced
24 audio is delayed in the receiver to allow synchronization to be
25 achieved.) As previously discussed, this synchronization is
26 accomplished in the MPEG standard by dropping or repeating video
27 frames.

28 In the device of FIGURE 28 incorporating the present
29 invention, the MPEG input signals are fed from the normal
30 compressor encoder circuits 160 in the customary mode of
31 transmission (tape, transmitter, receiver, cable, etc.) to a
32 modified adaptive decoder 190. The adaptive decoder 190 shown is

1 modified from a customary MPEG adaptive decoder in that the
2 adaptive decoder 190 has only slightly over a single field of
3 video memory 191, and the use of this optional memory is to allow
4 for an unusual override reset of the signal modification circuit
5 150 (as later described). (In contrast, the customary MPEG
6 demodulator has at least two frames of memory, which memory is
7 actively used for audio resynchronization.)

8 The video signal in this modified device is directed
9 through the adaptive decoder 190 to produce an output video
10 signal in the customary manner according to with MPEG standards,
11 except that it trails the audio signal by approximately two
12 frames (this due to the deletion of the audio to video
13 synchronization from the video signal path).

14 The audio input signals 10 are fed through the adaptive
15 decoder 190 to convert such signals to customary form. The audio
16 input signals 10 are, however, then passed through a signal
17 modification circuit 150 in order to add or subtract samples to
18 synchronize the audio to the video signals. This synchronization
19 is accomplished by adding or deleting samples in the audio input
20 signal 10 according to the invention. Thus, as the relative
21 delays of audio and video change, the audio delay time may be
22 adjusted, without pitch changes, to enable proper synchronization
23 with the video. This is preferred in that it occurs at a much
24 lower hardware/software cost than a video memory or memory system
25 would produce. This would normally be an intermittent procedure
26 accomplished after relative synchronization was lost, typically
27 during times of major video changes. The relative video delay
28 allows resynchronization without the introduction of
29 objectionable artifacts. For example, the unique number
30 transmitted every .7 seconds in the MPEG system could provide a
31 reference for automatic synchronization by altering the signal
32 modification circuit 150 to add or subtract samples as needed

1 under the control of the interface comparing logic 170.
2 The control of the audio delay may be either a feed
3 forward (fig 28) or a feed back arrangement (fig 29).
4 In the feed forward configuration, the time flags of
5 the video and audio which are output from their respective
6 decoders are compared to determine the amount of delay which the
7 audio needs to achieve synchronization with the video. This
8 delay is coupled to the audio delay control to cause it to change
9 to the desired amount. In this application, the audio and video
10 signals are fed through a compression encoder 250 subject to the
11 time flag 251 in the customary manner. However, on decompression
12 while the video signal 10 is fed through a customary rate
13 convertor 253, the audio signal 10 is fed through the signal
14 modification circuit 50 to resynchronize the signals. A
15 comparator 255 analyzes the video flag and audio flag to
16 automatically control the sample addition/deletion of the
17 modification circuit 50.
18 In the feed back configuration, the time flags of the
19 audio output from its decoder are delayed by the same amount as
20 the audio is delayed in the variable memory. The audio time flag
21 and audio may of course be delayed in the same, or separate
22 matching memories. The video time flag corresponding to the
23 output from the variable memory is compared to determine the
24 amount of synchronization error of the audio relative to the
25 video. This error is coupled to the audio delay control to cause
26 it to change to correct the error. In this application, the
27 audio signal 10 is fed to a modified signal modification circuit
28 50A, a circuit that actively acts on the audio flag in addition
29 to the audio signal 10. The comparator 255A then compares this
30 delayed audio flag to the video flag in order to control the
31 signal modification circuit 50A to resynchronize the audio output
32 to the video.

1 In this resynchronization, however, as previously
2 described in respect to FIGURES 17-19, there is a possibility
3 that very occasionally the reset control 65 in the signal
4 modification circuit 50 might not have operated near to the end
5 of an operative total delay length. In FIGURE 23, when this
6 would occur, the field memory would preferably be operated in
7 order to repeat a field, and thus allow for the forced resetting
8 of the signal modification circuit 50. In the embodiment shown,
9 this is provided by an override signal 151 from the signal
10 modification circuit 150 to the video decoder.

11 As a further improvement, it will be advantageous to
12 either compare time flags of multiple sound channels of a given
13 audio signal in order to correct any channel to channel phasing
14 and polarity errors which may exist (fig 30). One example of
15 such a system would be video surround sound audio having 5
16 channels corresponding to left front, right front, left rear,
17 right rear, and subwoofer. The channels would be compared to
18 each other to ensure that their relative phasing or timing are
19 kept correct, with any timing errors being used to control fine
20 phase adjustment of each controlled audio channel. In this
21 application, the various channels 1-5 would each be subject to
22 its own individual delay in the delay circuit 56B, with samples
23 added or subtracted therefrom based on a signal modification
24 circuit 50B. This circuit 50B and the delays are automatically
25 adjusted by the flag comparison circuit 255B. Feed forward could
26 also be utilized.

27 The control of multiple sound channel timing for any
28 multiple sound channel application may be implemented by itself
29 with the variable delay capability of the present invention.
30 This is especially true because of the precise delay control
31 which may be achieved in the present invention. Multiple sound
32 channel timing control is, however, quite cost effective.

1 Further, it is very useful to include such correction as an
2 additional capability of audio to video synchronization
3 circuitry. Another invention showing correlation of multiple
4 audio channels for applications where audio and video are
5 transmitted over different paths is shown in Cooper U.S. Patent
6 4,703,355 which is incorporated herein by reference with respect
7 to its prior art teachings and in particular, signal correlation
8 and generation of control signals responsive thereto.

9 The invention may be utilized in an entertainment or
10 other system to provide faster or slower than normal recording or
11 replay of audio, and if desired associated video. Other
12 information may be utilized as well, with the teachings herein
13 being just as applicable to storage or replay of any information
14 having a frequency parameter where it is desired to alter the
15 time duration without altering the frequency.

16 FIGURE 31 shows a system in which a physical storage
17 medium 300 along with its associated scanning mechanism is
18 controlled by the user by providing a varying reference to the
19 scanning mechanism. It is preferred that the physical storage
20 medium be a digital video disk such as a common optical CD device
21 which utilizes a spindle motor to rotate the storage medium,
22 which is the disk, and a laser and optical scanning head which
23 make up the scanning mechanism. It is preferred to provide the
24 servo mechanism for the spindle motor with a variable frequency
25 reference signal which is provided by a Numerically Controlled
26 Oscillator (N.C.O.) 305 whose frequency is controlled by the user
27 interface and control logic 310.

28 The user interface and control logic 310 also
29 interactively controls the optical scanning head position,
30 receiving positional data from the scanning mechanism (which
31 alternatively may be provided via the recorded data) to perform
32 start, stop, record, play, search and other functions normally

1 provided. In this manner the recording or playback of the audio
2 and/or video data may be controlled to take place at different
3 and variable rates. It should be noted that while the term data
4 is used to denote what is stored in the storage medium, that it
5 is not to be construed that this data is to be limited to digital
6 data. Data as used herein is simply meant to mean the
7 information which is stored in whatever form it may exist.

8 While this embodiment of the invention is preferred to
9 be a CD device, one skilled in the art will recognize from the
10 teachings herein that any storage device may be adapted to
11 implement the invention, including analog video disk recorders,
12 analog audio tape recorders, DAT recorders, video optical disc
13 recorders, video tape recorders, rotating magnetic disk recorders
14 (such as computer disk drives), film based recorders and
15 projectors, solid state memory including semiconductor memories,
16 charged coupled device memories, switched capacitor recorders,
17 and three dimensional solid memories such as laser addressed
18 crystal lattices. All of these storage device types have in
19 common a mechanical, electronic, optical or combination scanning
20 mechanism which selects where within the physical storage medium
21 the data is stored or read. It is by controlling the rate at
22 which this scanning mechanism operates that the rate of storage
23 or reading is made variable. The invention may be utilized with
24 record only, playback only or record and playback versions.

25 As one skilled in the art will understand from these
26 teachings, varying the rate of reading or writing may not be
27 successful over a very large range by simply causing the scanning
28 mechanism to operate at different rates. In virtually all
29 storage devices, the data is stored in a form which takes on many
30 analog characteristics. With the preferred optical disk medium,
31 the data is stored as alternating light polarization of a layer
32 of material. The data is read back by the laser beam which beam

1 is directed to an electro-optical sensor or converter thus
2 providing an electrical signal which varies in response to the
3 laser light. By changing the speed of the disk and scanning, the
4 frequency and intensity characteristics of the laser light are
5 altered, thereby altering the frequency and intensity
6 characteristics of the corresponding electronic signal.

7 In virtually all recording and playback systems, there
8 is required compensation circuitry to make up for nonlinear
9 characteristics of the system. These compensation systems are
10 critical to the proper recovery of the audio and video and are
11 included in the modulator 320A and demodulator 320 circuitry.
12 Unfortunately, the nature of these nonlinear characteristics is
13 dependent on the scanning speed, thus causing a serious
14 compensation problem which is overcome in the above system. Most
15 commonly, frequency response of the system changes in fashion
16 which is dependent upon the frequency of the data. Many systems
17 operate to detect the changes in the data rather than the data
18 itself. The sensors which are thus used most commonly respond to
19 the electrical, magnetic, electromagnetic, or optical flux from
20 the storage and scanning mechanism combination and have an output
21 which is proportional both to the magnitude and rate of change of
22 the flux. The demodulator 320 thus must compensate for the
23 change which compensation in turn must be altered as the rate of
24 change of flux is altered by the changing of the scanning speed.

25 The requirement to change the compensation caused the
26 demodulator 320 to be adaptive, and controlled by the user
27 interface and control logic 310 in order to properly demodulate
28 the audio and video at any of the continuously selectable
29 playback speeds. FIGURE 33 shows an adaptive filter network
30 which is operable to change the filter compensation to fit the
31 playback or record speed. The filter utilizes varactor diodes
32 350 to provide a voltage variable capacitance, thus changing the

1 filter frequency characteristics. The voltage which is applied
2 to the varactors is provided by a digital analog converter 360,
3 which in turn is loaded with the appropriate digital number for
4 the particular speed being used, which loading is accomplished by
5 the user interface and control logic 310. Linearization or
6 voltage mapping circuits 351 are provided at the input and output
7 of the filter and at the varactors 350 to compensate for any non-
8 linearities therein. In operation the filter operates to reduce
9 the high frequency content of the data signal to a proper level,
10 the amount of reduction depending on the speed of the data.

11 Returning to figure 31, as for any particular physical
12 storage medium which would be preferred, the proper design of
13 compensation at given fixed speeds is well known to those skilled
14 in the art. It is believed that from the teachings given herein,
15 those skilled in the art will also be capable of designing
16 compensation which is variable over a suitable range of
17 operation. In this manner the invention of the figure may be
18 practiced such that the operator may select any speed within a
19 range of speeds with the recording and playback of data of the
20 storage medium operating properly.

21 It should be noted that some existing audio tape
22 recording systems have the capability to change frequency
23 equalization of the audio signal as the tape speed is changed
24 from one discrete speed to another, for example from 7.5 IPS to
25 15 IPS. In addition, many of these tape recorders may playback
26 at continuously variable speeds to facilitate searching.
27 Applicant is unaware of any of these systems having continuously
28 variable equalizers to insure properly equalized audio at all of
29 the continuously selected speeds which the operator is capable of
30 selecting.

31 After the audio and video is demodulated by the
32 adaptive demodulator 320, it is required to pitch correct the

1 audio under control of the user interface and control logic 310
2 as by the circuitry described in the preceding figures, and to
3 convert the rate of the video to standard rates in order that it
4 may be viewed on standard viewing devices. The video rate
5 converters 330 are known in the art as frame synchronizers.
6 While it is possible for frame synchronizers to operate self
7 contained, improved operation and lower cost may be obtained by
8 providing the rate converter with information and control from
9 the user interface and control logic, and additional features
10 such as video special effects may be provided as well. The pitch
11 converter 340 is as set forth in this present application.

12 If it is desired to record at variable rates, the same
13 problems as described above for playback enter into the proper
14 modulation of audio and video before recording. Consequently it
15 is needed to provide an adaptive modulator 320A. In addition, it
16 may be desirable to provide a pitch corrector 340A and video rate
17 converter 330A on the record side of the device in order that the
18 recorded data appears as if it had been recorded at a particular
19 rate. One skilled in the art will recognize that a desired end
20 result of expanding or compressing a time segment may be achieved
21 by operating on the video and/or audio either when recording or
22 upon playback or both. In addition, there is no requirement that
23 both audio and video be operated on at the same time, as one may
24 be corrected on recording and the other upon playback.

25 A two way pitch shifter has been implemented with a
26 Star Semiconductor SPROC IC and is shown in FIGURE 20. The SPROC
27 IC is available from Logic Devices, Inc. of Sunnyvale, California
28 and is of type SPROC-1400-50PG132C. Information on the use of
29 this and similar ICS is available from Logic Devices, Inc.

30 The preferred embodiment would use type SPROC-1400-
31 50MQ144C, which functions similarly, but at a lower cost.

32 The block diagram FIGURE 26 is directly compatible with

1 the SPROC Development System Part Number SPPROClab™ version
2 1.25, P/N SDS-1001-03 with SPROClab version 1.25 patch B, P/N
3 SDS-1002-01B. Figure 26 is a schematic representation of digital
4 signal processing.

5 In this embodiment of the invention, the frequency
6 converter system is specifically designed for a stereo audio
7 source having a 20kHz input bandwidth. However, it should be
8 understood that the frequency converter system is equally
9 adaptable to systems of various input frequencies and bandwidths.
10 The audio input signals 10 are sampled at 48kHz sample rate. The
11 50MHz P/N SPROC-1400-50PG132C SPROC chip is used for processing.
12 Left and right channels are processed identically, and in
13 parallel. Some control blocks (or "cells" in the Logic Devices,
14 Inc. nomenclature) are common to both left and right.

15 Three basic operations are performed: stretch (or
16 expand)/interpolate or compress/interpolate, reset, and reset
17 timing control.

18 ST-INO 202 accepts Format 2 stereo input samples which
19 are provided by a Crystal Semiconductor CS5326 A-D Convertor.
20 Output 1 is the right channel, and output 2 is the left. This
21 discussion will concentrate on the left channel and common
22 processing.

23 Stretch cells ST1 200 and ST2 201 each perform the
24 stretch/interpolate or compress/interpolate functions in stereo.
25 Most of the time, only one is actually connected to the output.
26 Two are required during a reset operation, as will be described
27 below. ST1 200 and ST2 201 perform reads and writes to RAM
28 circular buffers 56, 57 in order to accomplish the stretch or
29 compress function.

30 Two way stretch cells are used at ST1 200 and ST2 201.
31 In the pitch increase mode, delay might start at 35 mS and
32 decrease until a crossfade reset event occurs. At reset, delay

1 is returned to or near 35 mS, and the process repeats. In the
2 pitch decrease mode, delay starts at or near zero, and increases
3 until a cross fade reset event occurs. At reset, delay returns
4 to near zero, and the process repeats. Thus, while in the pitch
5 decreasing mode some program material is discarded at a reset, in
6 the pitch increasing mode some program material is repeated. In
7 the pitch increase mode, ST1 200 and ST2 201 output stereo
8 samples at the 35 mS memory candidate reset point for splice
9 match testing. These samples, "OUTC" 203 and "OUTD" 204 of ST1
10 200 (203A, 204A) and ST2 201 (203B, 204B) cells, pass through
11 switches SW3 205 and SW4 206 so that those of the correct stretch
12 cell may be selected. If the pitch decrease mode is selected,
13 "OUTC" and "OUTD" produce samples of near zero delay.

14 An abrupt reset of a single stretch cell often results
15 in an audible click. In this design, a more gradual reset occurs
16 as follows. Suppose only ST1 200 is connected to the output.
17 Further suppose the pitch decrease mode is operative. At the
18 start of a reset, ST2's 201 delay is set to or near zero. At the
19 same time, a gradual fade from ST1 200 to ST2 201 is initiated
20 and performed by 207. At the completion of the fade, only ST2
21 201 is connected to the output. The delay through each stretch
22 cell continues to change during the fade operation. At the next
23 reset, the operation is reversed, and so on. This technique is
24 effective at suppressing reset clicks.

25 The left channel outputs of ST1 200 and ST2 201 connect
26 to the output via MFADE0 207. A ramp signal is applied to MFADE
27 207 to accomplish the fade. This ramp is formed by MMV1 211,
28 MMV2 212, MINUS3 217, and INT2 214. Depending on direction,
29 either oneshot MMV1 211 or MMV2 212 produces a pulse 3072 samples
30 (64ms) long. Integrator INT2 214 forms the ramp. Subtraction
31 cell 217 causes alternate ramps to be in different directions.
32 INT2 214 output takes values between 0 and 1.0. Ramp length of

1 64mS was determined empirically. Too short a ramp produces an
2 abrupt transition; too long produces an echo effect.

3 A reset is initiated only when the differences between
4 input and output slope and instantaneous amplitude are within
5 certain limits, in order to make the cleanest splice practicable.
6 Amplitude and slope match for the left channel are measured by
7 MINUS2 221; first difference cell DIFF2 222; and cells p1 223 and
8 p3 224. SW1 225 selects the appropriate stretch cell output. p1
9 223 or p3 224 produces an active low reset signal whenever the
10 magnitude at the cell input is below a certain threshold. These
11 thresholds are continuously scaled according to signal level and
12 slope. The intent is to require the same relative match,
13 independent of amplitude or instantaneous frequency. This
14 scaling is performed by SUM1 213; DIFF3 230; and, peak detectors
15 PD0 231 and PD1 232. SUM1 213 performs full wave rectification,
16 of each input, and sums the results to produce its output. PD0
17 231 and PD1 232 gains set the degree of match required.

18 Outputs from p1 223 and p3 224, as well as outputs from
19 the corresponding right channel cells p9 235 and p10 236, must
20 all be simultaneously low to enable a reset. Or gate OR1 229
21 performs this function. Additionally, cell p7 237 sets the
22 minimum time between reset events at 9600 sample periods (200mS).
23 Any reset inputs to p7 within the last 200 mS from a reset output
24 from p7 are ignored. The 200 mS value was empirically optimized
25 as a compromise between rapid warble like artifacts and loss of
26 repetition of program material. Minimum time between resets
27 could be caused to vary randomly about the 200mS value, to reduce
28 the periodicity of resets. Some artifacts are still detectable.
29 Cells p8 247 and OR4 248 have been carried over from previous
30 design iterations, but are not functional in this design.

31 P7 237 emits a one sample width active low reset pulse.
32 This is steered to the appropriate oneshot and stretch cells by

1 logic formed by threshold detector GT1 238; INV1 240; Or2 241;
2 and, OR3 242. Delay cells DELAY2 245 and DELAY4 246 are intended
3 to correct timing misalignments.

4 Cells that are specific to right channel operation are
5 DELAY3 249, SW2 250, MINUS4 251, SUM4 252, p9 235, p10 236, DIFF4
6 252, DIFF5 253, PD2 254, PD3 255, RECT5, and p11 256. p11 is not
7 functional in this design. Stereo output is accomplished by
8 parallel port output cells OUT0 257 and OUT1 258. Output
9 parallel data is subsequently converted to serial format by
10 hardware interfaced to the SPROCTM parallel port. This serial
11 data is then converted to 8X oversampling format by a Nippon
12 Precision Circuits Ltd. SM5813APT IC. The over sampled data is
13 passed to two Analog Devices, Inc. AD1862N digital-to-analog
14 converter ICS, to produce analog stereo audio output. Control of
15 pitch correction factor and reset point is accomplished by
16 changing the output levels of VR98 259 and VR99 260. To decrease
17 pitch by 9.09 percent, VR98 level should be 2 (reset point of 2
18 samples delay), and VR99 level should be 1.0. For no pitch
19 change, VR98 level should be 2, and VR99 level should be 0.0. To
20 increase pitch 10 percent, VR98 level typically would be 1680
21 (reset point of 1680 samples, or 35 mS, delay), and VR99 level
22 should be -1.1. AMP3 261 scales the pitch correction factor
23 output from VR99 260 and passes it to stretch cells ST1 200 and
24 ST2 201. The output levels of VR98 259 and VR99 260 may be
25 modified by the SPROC development system, both during the initial
26 building of the design, and during operation. Ideally, pitch
27 correction factor and reset point may be controlled by an
28 embedded microprocessor communicating with one of the SPROC
29 ports. Serial output cell OUT3 262 sends the fade ramp signal to
30 a PCM56 DAC on the development board. This signal is a useful
31 telltale of system performance. This port is not supported in
32 the production board hardware, but this signal could be sent to

1 the probe port (which will be supported) by modifying the SPROCTM
2 initialization code.

3 Left and right channels are reset simultaneously, and
4 must meet the reset criteria simultaneously. The lowest gain
5 possible for PDO 231, PD1 232, PD2 254, and PD3 255 should be
6 used. Experiments with program material showed that gains of
7 less than 0.1 (for example, 0.08) were too low. With gains of
8 0.08, excessive time between resets were regularly observed.
9 Program material tests at 9.09 percent pitch decrease mode, with
10 gains of 0.1, indicate that most resets occur within 250mS, and
11 that intervals beyond 300mS are rare (the corresponding memory in
12 the stretch cell would be one tenth these numbers; at 9.09
13 percent pitch decrease). These gains, as well as the other
14 parameters such as minimum reset interval and ramp slope are
15 easily changed in software.

16 The memories of ST1 200 and ST2 201 in FIGURE 20 are
17 arranged as circular buffers. Data is continuously written to
18 the inputs such that each buffer contains the most recent samples
19 for a period equal to the memory length. In fact, the contents of
20 each memory are the same, since each has the same input. In
21 addition, OUTC 203A and OUTC 203B output the same data. The same
22 is true for OUTD 204A and OUTD 204B. Therefore, an improved
23 embodiment would be obtained by combining ST1 200 and ST2 201,
24 and using a single memory. SW3 205 and SW4 206 would no longer
25 be required. It may also be possible to combine the functions of
26 OUTA with OUTC and OUTB with OUTD, respectively. A minimum of
27 two separate memory outputs would still be needed, of course, to
28 support the signal comparison and reset operations. Further code
29 savings could be obtained by eliminating the NDXIN and NDXOUT
30 outputs from ST1 200 and ST2 201, or a combined cell, since these
31 outputs are not used in this embodiment.

32 FIGURE 27 shows pitch correction integrated with the

1 delay function. The pitch corrector functions of FIGURE 25 are
2 essentially cascaded intact with the delay function, except with
3 the added ability to force or inhibit stretch cell 200 and 201
4 reset. Cell TAU0 263 operates directly on the input samples, and
5 produces delay. TAU0 263 changes delay in a manner identical to
6 stretch cell operation, but without resetting. TAU0 263 utilizes
7 external memory. Since pitch shift occurs during delay change,
8 TAU0 263 output is passed to ST1 200 and ST2 201 for pitch
9 correction. TAU0 263 also performs parallel port access for
10 stereo sample output and microcontroller interface. Stereo
11 output samples from MFADE0 207 are passed to TAU0 263 for output
12 via the SPROCTM parallel port.

13 Cell CNO 264 coordinates operation of the delay and
14 pitch correction cells. TAU0 263 reports its current delay to
15 CNO 264. CNO 264 reads stretch cell index values. The indices
16 from the active stretch cell are selected by SW5 265 and SW6 266.
17 CNO 264 computes the current stretch cell delay, and adds the
18 TAU0 263 delay to determine total delay. This total delay is
19 passed to TAU0 263 for parallel port output to the micro-
20 controller.

21 Target delay is read from the microcontroller via TAU0
22 263. If total delay equals target delay, CNO 264 holds TAU0 263,
23 ST1 200, and ST2 201, by writing zero to the slew factor inputs
24 of those three cells, and inhibiting stretch cell reset.

25 If total delay differs from target delay by more than
26 20 mS, the following sequence of events occurs. First, the
27 stretch cells are initialized. If the delay change direction
28 should be opposite of the previous change, it is likely that the
29 initial stretch cell delay is too far removed from the
30 appropriate reset point. CNO 264 sweeps the reset point values
31 in the vicinity of the nominal for a period of 0.5 Sec, enabling
32 a high probability of a splice. When this splice occurs, the

1 stretch cell becomes initialized without an abrupt transition.
2 Then, CN0 264 outputs complementary slew values to TAU0 263, ST1
3 200, and ST2 201. This produces delay change and pitch
4 correction at a ten percent rate. ST1 200 and ST2 201 delay the
5 slew factor by the same amount as the audio, to maintain temporal
6 registration between the two. The total delay change occurs
7 primarily during fades, because of the pitch corrector reset
8 action. Delay change during each fade is generally of slightly
9 more than 20 mS in size. When the total delay becomes within +/-
10 20 mS of the target, the stretch cells are held, and TAU0 263
11 slews at a 0.2 percent rate, without pitch correction, until the
12 target is reached. If TAU0's 263 delay reaches zero before the
13 target is reached, TAU0 263 is held, and the stretch cell delay
14 is decreased at a 0.2 percent rate, without pitch correction,
15 until the total delay is correct.

16 For delay changes of 20 mS or less, the delay slews at
17 a 0.2 percent rate, without stretch cell initialization or pitch
18 correction.

19 The minimum delay target is one sample (1/48000 Sec.),
20 not counting data converter decimation or interpolation filter
21 delay. Dump mode is enabled by requesting zero delay. In dump
22 mode, TAU0 263, ST1 200, and ST2 201 are reset to minimum delay
23 and held. Requesting a nonzero delay target causes normal
24 operation to resume. In the present embodiment, control via the
25 SPROCTM development system is substituted for microprocessor
26 control.

27 In FIGURE 27 ST1 200 and ST2 201 could also be combined
28 in a manner similar to that described for ST1 200 and ST2 201 of
29 FIGURE 26. As before, SW3 205 and SW4 206 would not be needed.
30 In a combined stretch cell, only a single output NDXIN would be
31 required, which would also eliminate SW5 265.

32 Further reduction in code would be obtained by

1 combining ST1 200 and ST2 201 not only with each other but also
2 with memory cell TAU0 263. A single memory would then be used.
3 In both FIGURE 26 and FIGURE 27, a smoother fade ramp could be
4 obtained by using a raised cosine function, instead of a linear
5 ramp. In an improved embodiment, a watchdog timer function would
6 be incorporated into the hardware and code.

7 The preferred embodiment of the present invention may
8 be modified without deviating from the invention as claimed.

9 For example, the preferred embodiment is described as
10 operating on the input signal, a signal which is being produced
11 at a first speed, to produce the output signal, which output is
12 subsequently clocked at the second speed to provide the same
13 frequency based information. It would be possible to modify the
14 order of conversion without deviating from the invention as
15 claimed. For example, one could modify the frequency conversion
16 system of the present invention to create a second plurality of
17 signals clocked at different speed prior to frequency conversion.
18 This could occur, for example, on a taped system operated at a
19 higher or lower speed than normal to produce a signal in need of
20 frequency conversion. It could also occur on any type of signal
21 wherein the signal is stored on a disk, record, tape, computer
22 RAM memory, or otherwise in either a digital or analog form,
23 which signal is capable of being operated at something other than
24 real time speeds (both faster or slower). In this modified
25 device, the input signal would be reproduced at the output
26 signals' speed in order to create a version of the second
27 plurality of signals. An example of this would be to speed up an
28 audio tape recorder to produce a pitch changed version of the
29 audio stored thereon. At this time, the frequency converter
30 system of the present application would act upon this sped up
31 version of the second plurality of signals in order to modify the
32 number of samples therein to meet the requirements of the new

1 clock speed and thus produce the pitch shifted output signal. No
2 further memory would be needed if the sampling rate was high
3 enough. In the example audio tape recorder, samples would be
4 added in order to lower the pitch of the output signal to match
5 the pitch of the input signal originally recorded on the tape
6 recording, and thus produce a output signal having a frequency
7 substantially the same frequency as the input signal. The
8 frequency converter of this invention can therefore operate
9 before, during or after the clock shift of the input signal.
10 Similarly, the clock shift can be upwards (compression), downward
11 (expansion), or the same as (dropout compensation, profanity
12 dump) at any time during recording, storage, and/or replication
13 of the input signal.

JPS > A2
14 It is envisioned that other known techniques, such as
15 homomorphic signal processing, subband coding, Fourier
transformations, power spectrum *estimation*, correlation, or
16 *transformations*, power spectrum *estimation*, correlation, or
17 measurement of relative second or higher order differences, could
18 be used or adapted to improve the signal comparison. For example,
19 homomorphic deconvolution, followed by linear filtering, may be
20 applied to speech signals to separate pitch and other
components,² *components*,². Separated parameters could be respectively
21 compared. As another example, in subband coding a speech, image,
22 or other waveform is divided into several frequency bands, where
23 each band is coded separately. Individual subband components
24 could be respectively compared. As a further example, spectrum
25 amplitude and/or phase components as resolved by Fourier
26 transformation could be compared. In the case of correlation,
27 signals could be compared over some length considerably larger
28 than that of the comparison used in the present embodiment.
29
30 It is envisioned that in an improved embodiment
31 techniques such as homomorphic deconvolution, subband encoding,
32 or Fourier *transformations*² could be used, with suitable

1 modification, prior to the pitch shifting operation, to provide
2 signal component separation. The pitch conversion would then be
3 applied to one or more of the separated signal components. As a
4 particular example, homomorphic deconvolution, followed by linear
5 filtering, followed by the inverse to the homomorphic
6 deconvolution, may be applied to a speech signal to separate
7 pitch from other components. The described invention could be
8 applied to the so obtained pitch signal. Next, the frequency
9 converted pitch signal would be suitably recombined with the
10 other components. It is known that the representation of speech
11 in parametric form allows a modified pitch contour to be applied
12 to the data.
a data

13 It is also envisioned that data compression techniques
14 would be advantageous. For example, linear predictive coding
15 applied to a speech or other signals reduces the data rate
16 required to represent the waveform. Likewise, subband coding
17 applied to speech, video, or other signals reduces the data rate
18 required to represent the waveform. Narrow band voice
19 modulation (NBVM) techniques reduce the occupied bandwidth of a
20 speech signal, allowing a lower sample rate to be used.
21 Operating on compressed data would reduce the described
22 invention's memory and signal processing hardware requirements.

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3 Figure 6 show Data Manager and Program Data Processor
4 implemented by a Computer Processor Unit, and Data Storage for a
5 single program data stream. The data stream, which may have
6 embedded information is coupled to a Embedded Information
7 Recovery Circuit and to a FIFO. The FIFO is provided to
8 temporarily store incoming data while the Embedded information
9 (if any) is recovered and acted on by the Computer Processor
10 Unit. Embedded information may contain program related
11 information such as program type, air date and time, source or
12 other information for the present or future programs which the
13 user would find useful in determining the desirability of using
14 or storing the program. For example, if the user desires to store
15 sports highlights programs and the type of program (sports
16 highlights) is carried as embedded information, the Computer
17 Processor Unit will receive this information and direct the data
18 storage to store the data carrying the program. When data is to
19 be stored, the Computer Processor Unit selects a program address
20 which the Data Storage uses to store the program. The Computer
21 Processor Unit may either tell the Data Storage what address to
22 use, or may receive the address used therefrom. It is preferred
23 that the Computer Processor Unit keep track of all address
24 information and select an appropriate address, giving that
25 address to the Data Storage. The Computer Processor Unit also
26 stores the information relating to the program, such as date,
27 time, program name, program type, length of program, etc. along
28 with the location of the program in the Data Storage, in order
29 that the user may be informed of this stored information upon
30 request, and in order for the Computer Processor Unit to properly
31 manage storage, reading and overwriting of the data which is
32 stored. The Computer Processor Unit also selects either incoming

1 data or stored data to be coupled to the MPEG decoder which
2 decompresses the data stream into digital video and audio data
3 streams. The video and audio data streams are then coupled to
4 the User Display Interface circuit, which coupling may be direct
5 or via the Time Compression and Expansion Artifact Removal
6 circuit, under control of the Computer Processor Unit. The User
7 Display Interface converts the digital audio and video data
8 stream to proper form for use by the User Display (if necessary)
9 and in addition combines user messages of audio and video type
10 from the Computer Processor Unit with the data streams which are
11 coupled to the User Display. The Computer Processor Unit
12 controls the selection of programs to be read out of Data Storage
13 by providing proper Read Program Address, and also controls the
14 playback or read speed of the program in response to the users
15 wishes. In the event of playback other than normal, the
16 uncompressed audio and video are coupled through the Time
17 Compression And Expansion Artifact Removal circuit. This circuit
18 operates to remove pitch artifacts in the audio and motion
19 artifacts in the video by use of the invention described in
20 copending U.S. Patent Application serial number 089,904. While
21 the above storage system has been described with respect to the
22 preferred normal rate storage and variable rate reading, it is of
23 course possible to reverse the situation with variable rate
24 storage and normal rate reading in order to perform time
25 compression and expansion in those systems where there is control
26 of the incoming data rate. In addition, while it is preferred to
27 store MPEG compressed data for reasons of memory economy, it is
28 also possible to store uncompressed program data. The Computer
29 Processor Unit also serves to manage the interaction with the
30 User via communications with the User Remote and messages
31 provided on the User Display. The Computer Processor Unit
32 provides control of the Data Storage to accommodate the Users

1 wishes as well as providing and maintaining management of all of
2 the data related to the stored programs and any programming guide
3 information which is received via other services or the Program
4 Data Stream.

5 Although this invention has been described in its
6 preferred form with a certain degree of particularity, it is
7 understood that the present disclosure of the preferred form has
8 been made only by way of example and that numerous changes in the
9 details of construction and the combination and arrangement of
10 parts may be resorted to to provide equivalent functions and
11 elements of the invention without departing from the spirit and
12 scope of the invention as hereinafter claimed. For example, the
13 FIFO in figure 6 is used to allow processing of the program
14 information by the CPU before accessing the data stream. This is
15 necessary due to the contemporaneous transmission of the program
16 information and corresponding data. With systems having advanced
17 program information, this FIFO would not be necessary. Other
18 changes are also possible.

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